VFCB Pulse Width Modulation scheme for a new three phase MLI with reduced device count and dc voltage sources

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ABSTRACT

Multilevel Inverters are a new family of converters for dc-ac conversion for the medium and high voltage applications. The paper arbitrates the theory of a variable frequency carrier band pulse width modulation (VFCBPWM) strategy to generate the firing pulses for the switches in a three phase multilevel inverter (MLI). The operation pronounces the benefits of a VFCBPWM technique to minimize the utilization of switches amongst the different levels of the MLI and leave way for lowering the total harmonic distortion (THD) of the output voltage . The modulating mechanism further enables a significant rise in the fundamental component of both the output phase and line voltage. The usage of comparatively lesser number of carriers in the method of producing the switching pulses serves to improve the output voltage spectrum. The MATLAB based simulated response ordains the flexibility of the choice of a target voltage and augurs to operate the load in accordance with the utility requirements. The hardware based investigative study attempts to validate the simulated results . The results enliven its ability for its use in industrial entities in light of its resurgent claim to obviate the performance of multicarrier pulse width modulation (MCPWM) strategy.

Keywords:

INTRODUCTION

Over the last few decades, multilevel inverter (MLI) topologies have gained popularity in industrial application because of the superior power quality compared to its conventional two-level counterpart. MLI is an attractive topology for high voltage DC to AC conversion [1]. The theory of MLI relates a power conversion strategy in which the nature of the voltage forms steps to bring the output closer to a sine wave and thereby reduce the total harmonic distortion .

The MLIs generate stepped output voltage by a proper arrangement of power electronic switches and either isolated or non-isolated dc voltage sources. The increase in the number of levels enables the output voltage to become closer to a sinusoidal pattern

and facilitate to lower the distortion [2]. The MLIs attempt to reduce the stress on the switching devices through its operational flexibility to follow a reduced path for the current and the presence of lower level voltage sources.

The MLI technology appears to be a very important alternative in the area of high power medium-voltage control and offer a much better performance over the traditional two-level inverters in terms of reduced total harmonic distortion, lower switch ratings, lower electromagnetic interference and higher dc link voltages. It creates an ability to synthesize waveforms and extract a better harmonic spectrum with less THD for the output voltage [3]. The stepwise output voltage heaves out the need for filters and attaches a capability to operate on low and high switching frequencies.

For low and medium voltage/power applications, MLI find their applications in almost every field of electrical engineering including renewable energy systems, HVDC applications, distributed generation (DG) system, industrial drive applications, uninterruptible power supplies, etc [4]–[6]. They are widely used in drives and other allied areas in industries. The fundamental MLI topologies include diode-clamped, flying capacitor and cascaded H-bridge structures continue to support medium and high-power industrial applications , still the device count becomes significantly high with the rise in the number of voltage levels.

The trend revolves around the use of reduced switched count configurations that perceive paths for the flow of current from a lesser number of power sources and still allow achieving the desired number of levels. However it envisages the usage of suitable PWM strategies to reach at a quality output voltage.

A novel topology of single phase Cascaded Multilevel Inverter (CMLI) was proposed to offer an optimised DC source utilisation, reduced switch count and curtailment of active switches in the conduction path [7].The proposed design was tested for its practicability by simulations in MATLB/Simulink and results was verified by experimental set up of a scaled prototype single-phase model.

In cascaded H-bridge multilevel inverter, a variable frequency inverted sine PWM technique was modelled. The analysis of conventional triangular PWM inverter and inverted sine PWM inverter using constant and variable switching scheme was done in MATLAB Simulink and verified experimentally by FPGA Spartan 3E processor[8].

Three PWM methodologies that include constant switching frequency, variable switching frequency and phase shifted PWM was explained for minimizing the output

voltage THD of the MLI .The simulation results was validated through the use of FPGA based prototype [9]. A variable frequency carrier band PWM method was proposed for switching the power devices in the cascaded MLI [10]. The simulation results was presented to bring out its ability of reducing the harmonics at lower switching frequencies.

Despite the continuing developments in the MLI technology, still there exists further need to reduce the number of power switches in different operating modes and evolve measures to lower the THD of the output voltage through the choice of an appropriate PWM strategy.

PROBLEM FORMULATION

The primary effort orients to examine the use of a variable frequency carrier band (VFCB) modulating mechanism for producing a variable voltage from a three phase series parallel switched cascaded MLI (SPSWCMLI). The formulation lays significance to eliminate the higher frequency components in order to lower the THD of the output voltage. It evaluates the performance of a VFCBPWM strategy with much lower number of carriers for providing a variable voltage to operate the three phase RL load [11]. It involves the use of field programmable gate array (FPGA) based prototype to substantiate the simulation results and erudite the merits of the formulation

POWER MODULE

The attempt revolves around the design to develop a new three phase series parallel switched MLI topology with the number of cells in accordance with the number of levels to support the power requirements of the load connected across the outer H-bridge of the proposed MLI. It falls in the category of cascaded MLI and ventures to reduce the number of power switches in the path for the flow of current.

The generalized nature of the structure exhibits its versatile capability to acquire the desired number of output voltage levels through an increase in the number of cells. The fundamental focus extends to derive a nearly sinusoidal output voltage with minimum number of active devices and provide lower THD levels across the operating range. The generalized structure of the MLI shows in Fig.1 and it integrates the modular cells with a bidirectional switch across each of them together with a H-bridge in each phase to provide the specified power for the RL load. A dc voltage source, two bidirectional and one unidirectional switch in the central limb forms each cell.

The dc voltages in the cells pick on equal magnitudes for the three phases to realize a symmetrical output voltage waveform. The letters (S_{a1}…. $S_{a(4k)}$), (S_{b1}…. $S_{b(4k)}$) and (S_{c1}…. $S_{c(4k)}$) represent the active devices in each phase respectively and the unidirectional switches (S_1 to S_4) , (S_5 to S_8) and (S_9 to S_{12}) constitute the H-bridge inverters and k stands for the number of cells in the topology.

MODES OF OPERATION

Fig.2 displays the section of the power module of the proposed nine-level MLI relating to Phase A and it engages the bidirectional switches S_{a1},S_{a2},S_{a4},S_{a5},S_{a6},S_{a8} and the unidirectional switches S_{a3},S_{a7},S_1,S_2,S_3,S_4 to allow the current to flow in Phase A. The use of bidirectional devices allows avoiding the passage of circulating current within the cell. Similarly the switches S_{b1},S_{b2},S_{b4},S_{b5},S_{b6},S_{b8} and S_{b3},S_{b7},S_5,S_6,S_7,S_8 and S_{c1}, S_{c2}, S_{c4}, S_{c5}, S_{c6}, S_{c8} and S_{c3}, S_{c7}, S_9, S_{10}, S_{11}, S_{12} carry the power in the other two phases respectively.

The connection diagrams seen in Figure 3 and 4 explain the modes of operation for the nine level MLI to generate $+4V_{dc}$ and $-4V_{dc}$ for the phase A output and the entries in Table 1 relate to the switches involved in each operating mode for the first phase of the three phase MLI. The Fig.5 compares the number of dc sources and number of power switches required to obtain increasing levels of output voltage per phase for both the proposed SPSWCMLI and the cascaded H-bridge multilevel inverter (CHBMLI) to establish the reduction in the switch count and brings out the benefits of the proposed three phase MLI topology. It follows that the number of active switches for increasing levels of per phase output voltage in the proposed MLI increases in accordance with the relation 4k+4 and 8k for the CHBMLI.

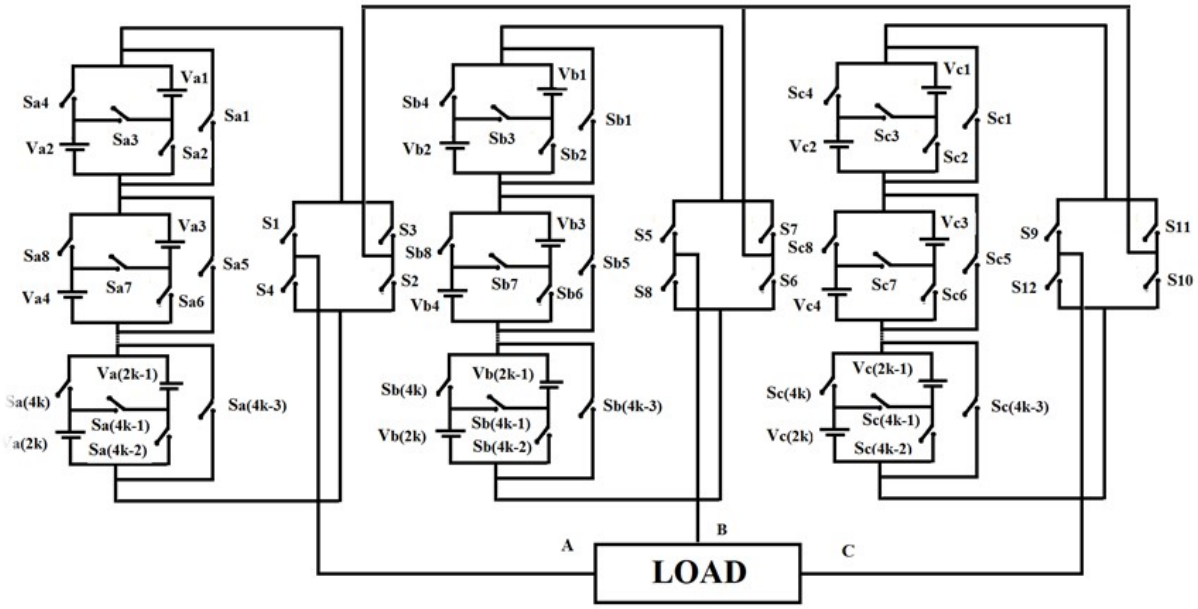

Figure 1 Generalized structure of proposed three phase SPSWCMLI

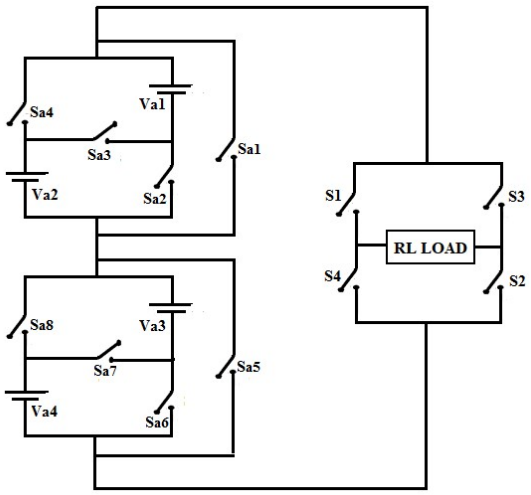

Figure 2 Proposed MLI topology for nine-level output for Phase A

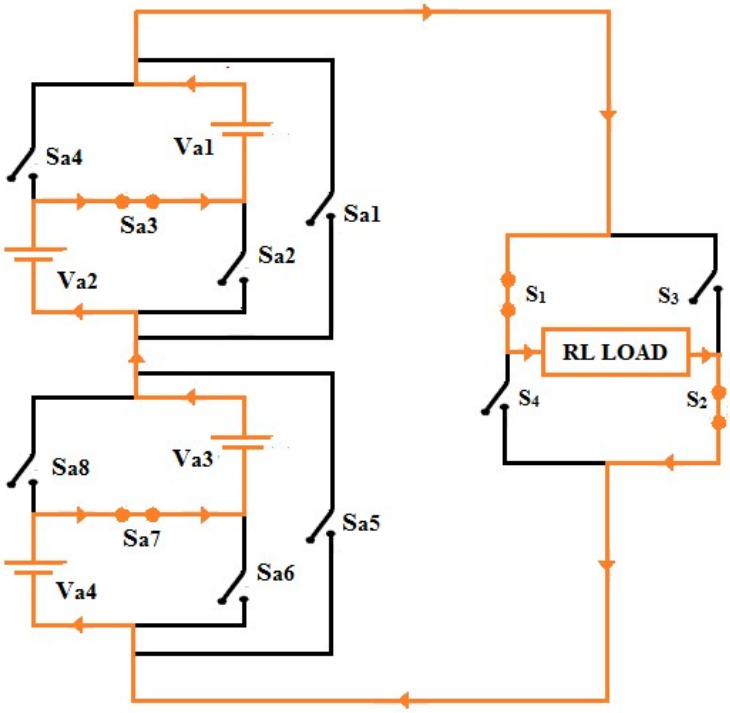

Figure 3 Modes of operation for +4V_{dc}

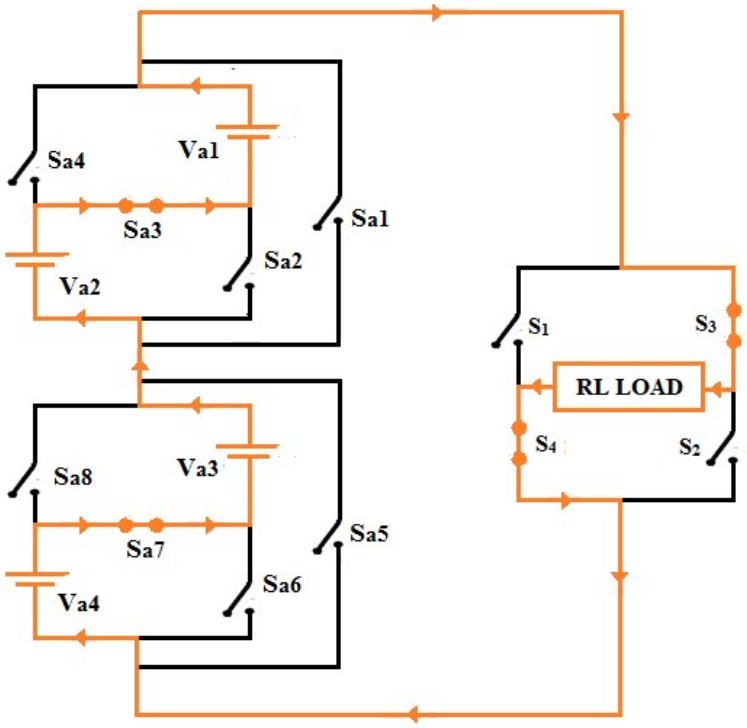

Figure 4 Modes of operation for –4V_{dc}

Table 1 Conduction Sequence of nine level operation for Phase A

Output Voltage Levels	Conduction of Switches											
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}	S_1	S_2	S_3	S_4
$+V_{dc}$	√					√		√	√	√		
$+2V_{dc}$	√						√		√	√		
$+3V_{dc}$		√		√			√		√	√		
$+4V_{dc}$			√				√		√	√		
$0V_{dc}$	√				√				√		√	
$-V_{dc}$	√					√		√			√	√
$-2V_{dc}$	√						√				√	√
$-3V_{dc}$		√		√			√				√	√
$-4V_{dc}$			√				√				√	√

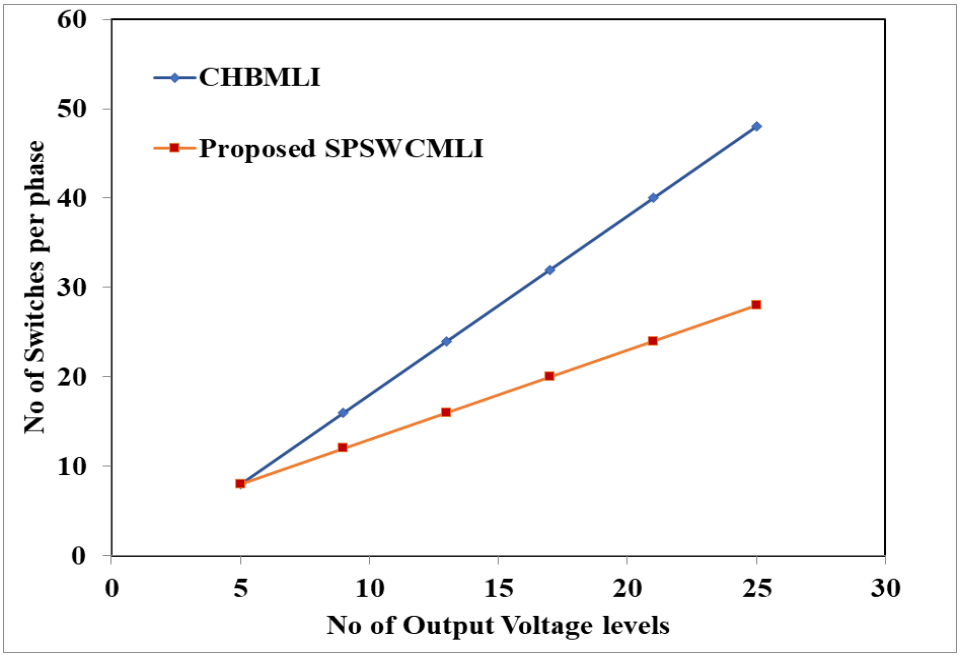

Figure. 5 Comparison of Proposed SPSWCMLI and CHBMLI

VARIABLE FREQUENCY CARRIER BAND PULSE WIDTH MODULATION STRATEGY

The effort owes to articulate the generation of PWM pulses in order that it enables the MLI to synthesize the output voltage in the form of a nearly sinusoidal shape .The approach orients to rearrange the frequency spectrum and assuage the reduction in THD levels through an increase in fundamental component[12]. The operation of a MLI depends to a large extent on the efficiency of the PWM scheme in being able to offer an enhancement in its performance. The influence of the nature of the carrier wave admonishes the capability to usurp a fresh scope for rearranging the higher frequency components of the output voltage.

The theory urges to employ a variable frequency carrier signal to leave way for varying the frequency of the carrier based on the slope of the modulating wave in each band. With identical carrier frequency for all the levels, the top and bottom levels experience more switching than the intermediate levels []. However the variation in the carrier frequency of each band enables to change the time duration that the reference waveform dwells in the carrier band and brings in measures to balance the switching action.

It requires (m-1)/2 carriers to implement a m-level inverter and augurs the difference between the carriers to be displaced by a dc offset. Besides the choice of the variable frequency carriers of the same magnitudes ensure that each band belongs to a different frequency range.

The algorithm enables the pulses when the amplitude of the modulating signal becomes greater than that of the carrier signal. The number of switching per modulation cycle (t) in each level of the inverter depends on the carrier frequency for that level and the duration of time that the reference waveform dwells within the levels corresponding time band. If the carrier frequency for all the levels remains identical, the top and bottom levels experience more switching than the intermediate levels.

The philosophy allows to vary the carrier frequency of each band based on the time duration that the reference waveform dwells in the carrier band in order to balance the switching action. Using the amplitude symmetry of the sine wave about the time axis, the band crossing times, where the reference waveform crosses from one band to adjacent band can be calculated.

The band dwell times in radians (starting at the band adjacent to zero axis) is determined as

$$t_{band_n} = 2(t_{n+1} - t_n) \tag{1}$$

$$\text{where} n = 0,1,2,3,.....,\left[\frac{m-1}{2}\right] \tag{2}$$

Because of the symmetry of the sine wave about the zero axis, the bands below the zero axis relate as

$$tband_{-n} = tband_n \tag{3}$$

The relation between the number of switching per bands, N_{sw_n} ,and the frequency ratio m_{f_n} ,for each band n of an inverter can be expressed as

$$m_{f_n} = \frac{\pi.N_{sw_n}}{tband_n} = \frac{\pi.N_{sw_n}}{2(t_{n+1} - t_n)} \tag{4}$$

The frequency ratio for each band can be set such that each level in the inverter contains approximately the same number of active device switching per cycle for all the levels. The hybrid frequency is calculated from the above equations to compute the variable frequencies for the carrier signals.

The carrier based PWM techniques with multiple carriers include the following categories phase disposition (PD), alternative phase opposition disposition (APOD) and carrier polarity variation (CPV). However the PD based approach throws a higher preference owing to the fact that it compares the carrier signals of the same frequency, amplitude and phase with a dc offset that occupy different levels in a single sine modulating signal and tends to provide load voltage and current with lower harmonic distortion [15].

The alignment of the reference and the carrier wave for the PD based constant frequency pulse width modulation (CFPWM) and variable frequency carrier band pulse width modulation (VFCBPWM) seen in Figs.6 and 7 relates to the PWM process for the switches in Phase A and ensemble the same procedure for the other two phases.

The combinational circuits operate to include the superimposition of the variable frequency triangular carrier waves with the sinusoidal reference in Fig.8 and derive the PWM pulses for the power devices in the proposed MLI for Phase A and incorporate a similar arrangement for the switches in the other two phases. The theory be-hives the philosophy of firing pulse generation for different modulation indices and incites the merits through a reduction in the levels of the THD.

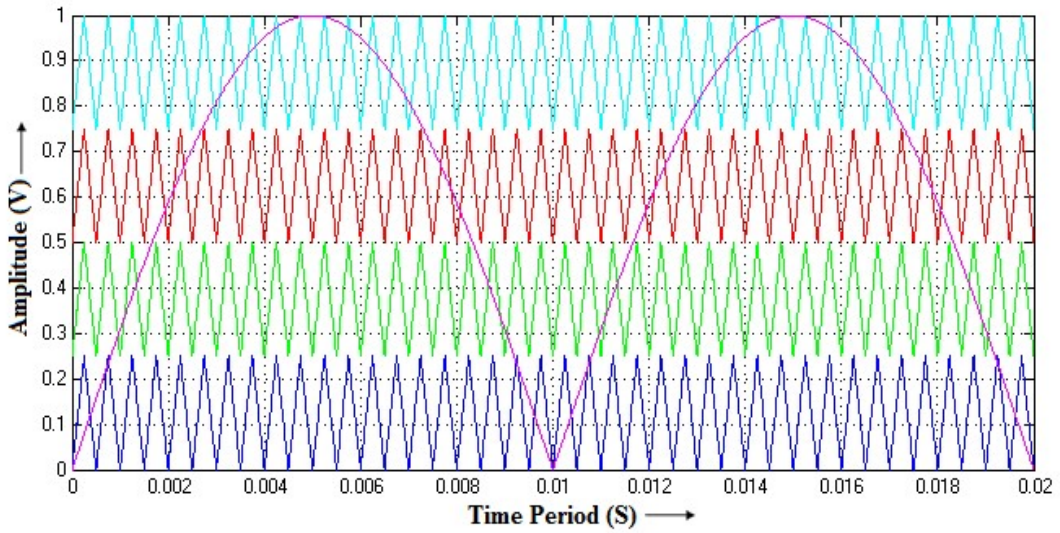

Figure 6 Reference and Carrier arrangement of PD MCPWM for Phase A

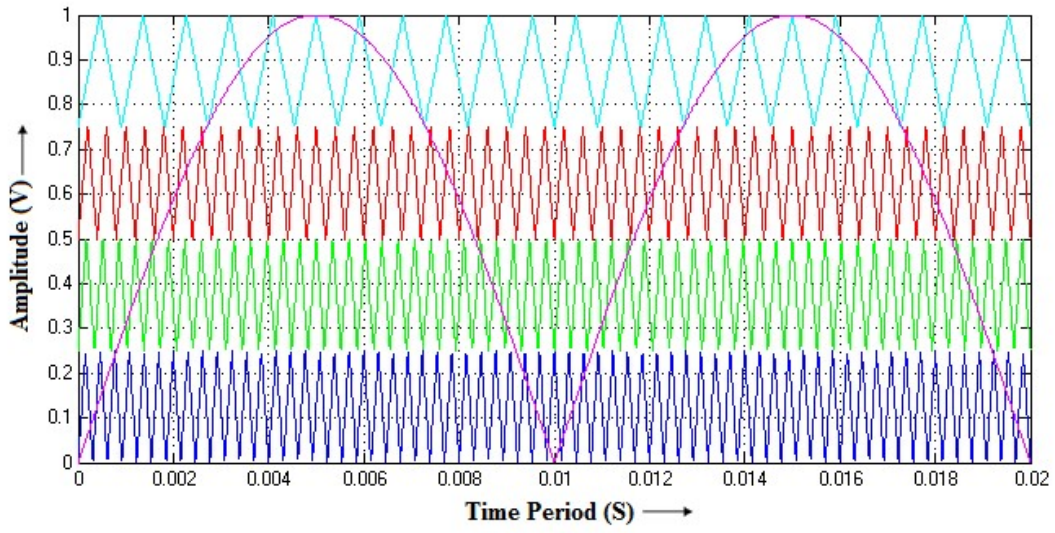

Figure 7 Reference and Carrier arrangement of PD VFCBPWM for Phase A

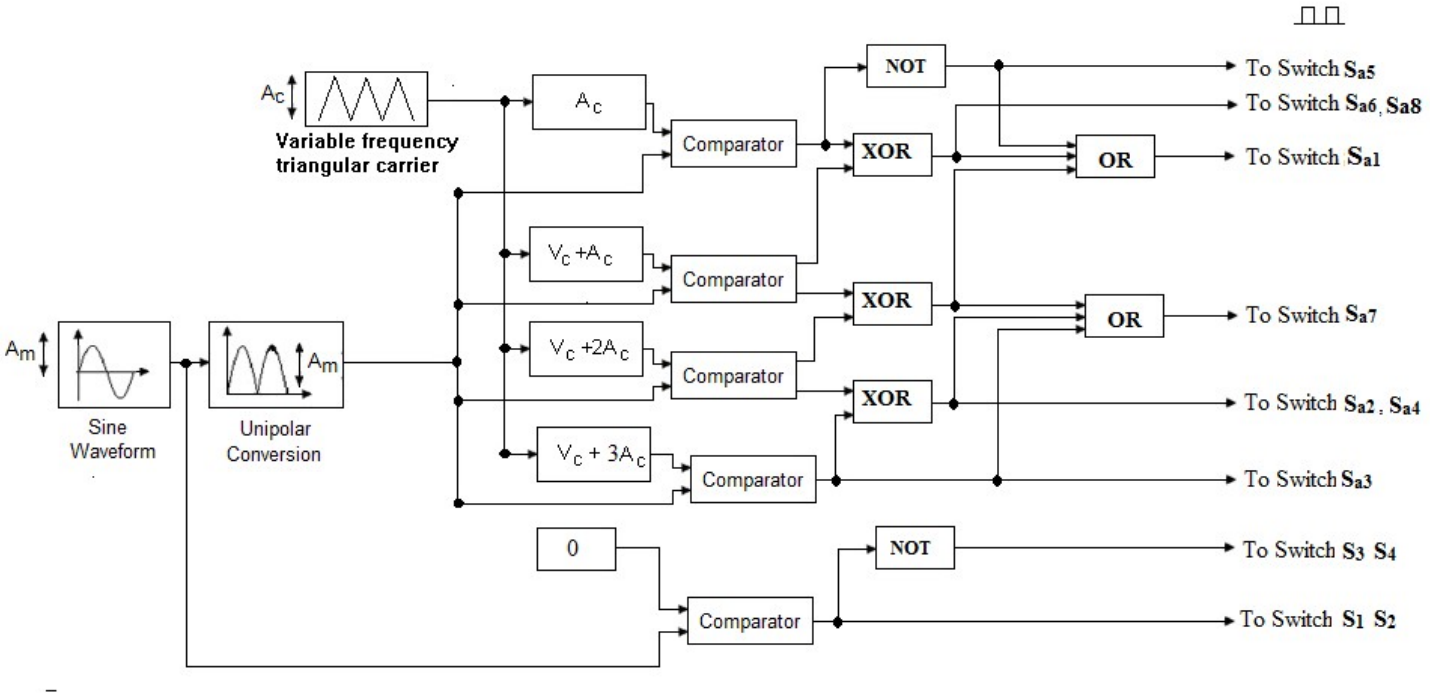

Figure 8 Generation of VFCBPWM pulses for Phase A

SIMULATION RESULTS

The emphasis relates to acquire a sinusoidal variable voltage for generating 415 volts, three phase output in accordance with the specific load requirements. It attempts to investigate the performance of the VFCBPWM strategy on the new three phase SPSWCMLI supported with identical magnitudes of 90 volts for the rectified dc voltage sources in both the cells through the MATLAB/Simulink platform to offer a nine level output for the RL load.

The output phase and line voltage waveforms and their respective THD spectra displayed in Figs 9 through 16 corresponding to Phase A at a modulation index of 1 and a chosen resistive-inductive load of 100 ohms and 150 mH respectively obtained using the MCPWM and VFCBPWM with a carrier frequency of 2 kHz respectively to elicit the advantages of both the new SPSWCMLI topology and the VFCBPWM scheme.

From the Figs 9 and 10,it is very clear , the constant frequency carrier based PWM increases the switch utilization in multilevel inverters. Thus, the proposed variable frequency carrier based PWM is to balance the switching duty among the various levels in inverters. The fundamental values and the THD indices obtained for the operating range of modulation indices seen in Figs 17 and 18 through bar and line diagrams respectively for the Phase A voltage. The Table. 2 shows the THD indices for the line voltage over the range of modulation indices and forges the fact that the VFCBPWM accrues the ability to eliminate the higher frequency components of the output voltage more effectively than the MCPWM.

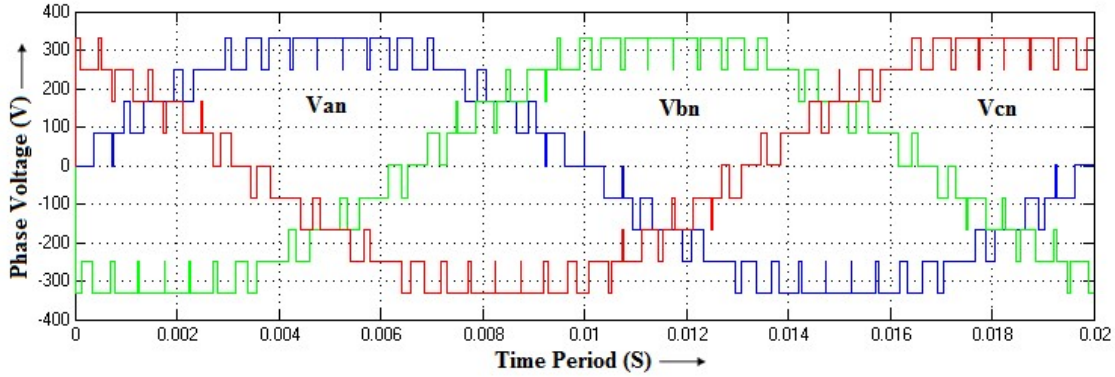

Figure 9 Phase voltage waveform for MCPWM

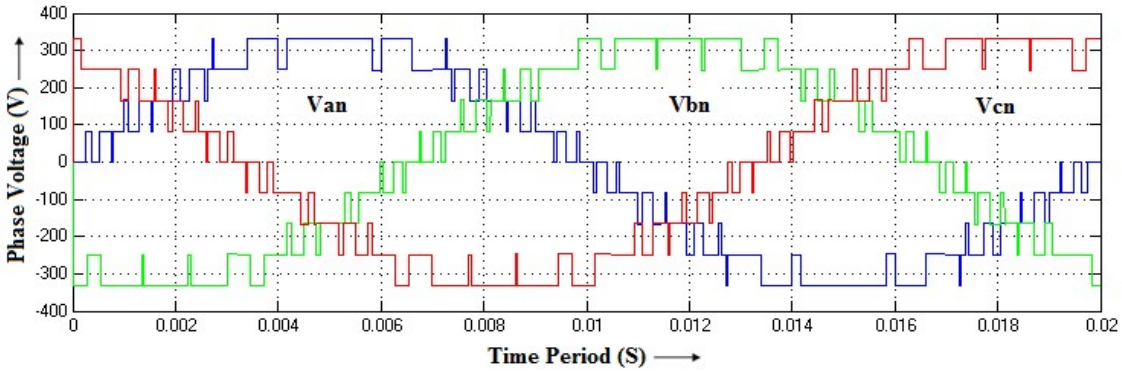

Figure 10 Phase voltage waveform for VFCBPWM

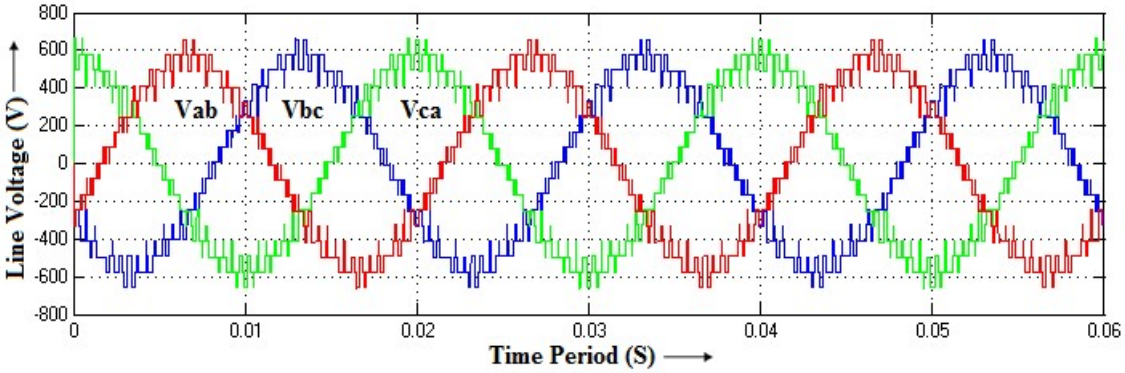

Figure 11 Line voltage waveform for MCPWM

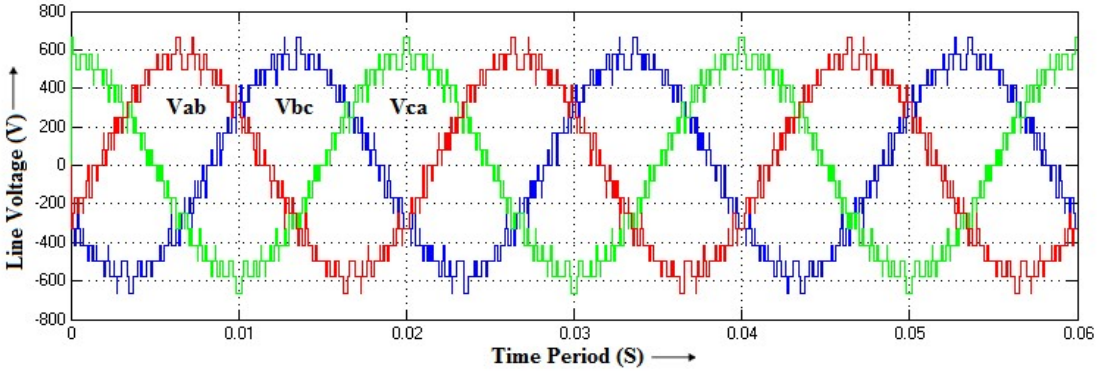

Figure 12 Line voltage waveform for VFCBPWM

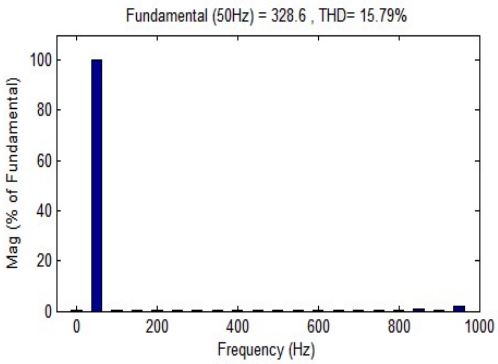

Figure 13 Phase voltage spectrum (V_a) for MCPWM

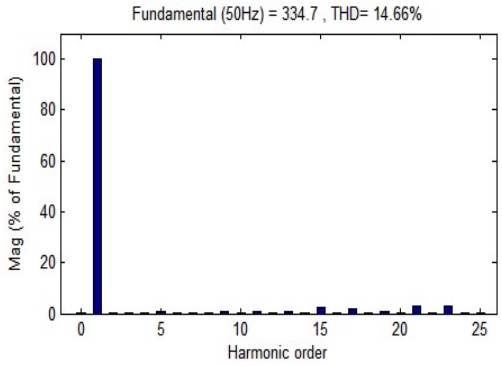

Figure 14 Phase voltage spectrum (V_a) for VFCBPWM

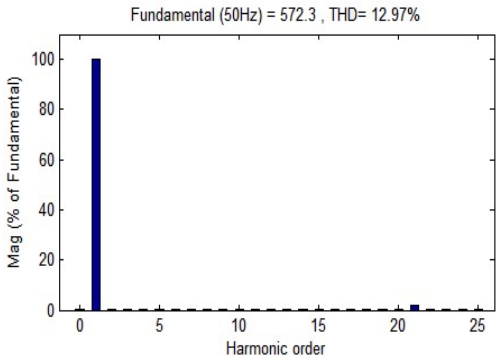

Figure 15 Line voltage spectrum (V_{ab}) for MCPWM

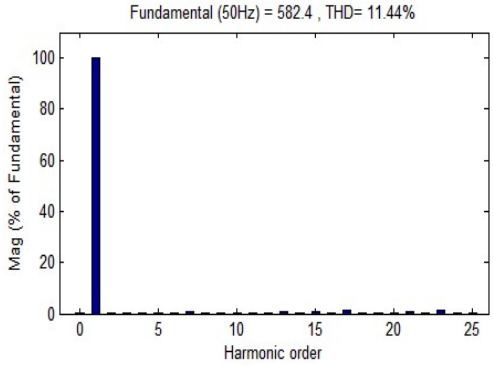

Figure 16 Line voltage spectrum (V_{ab}) for VFCBPWM

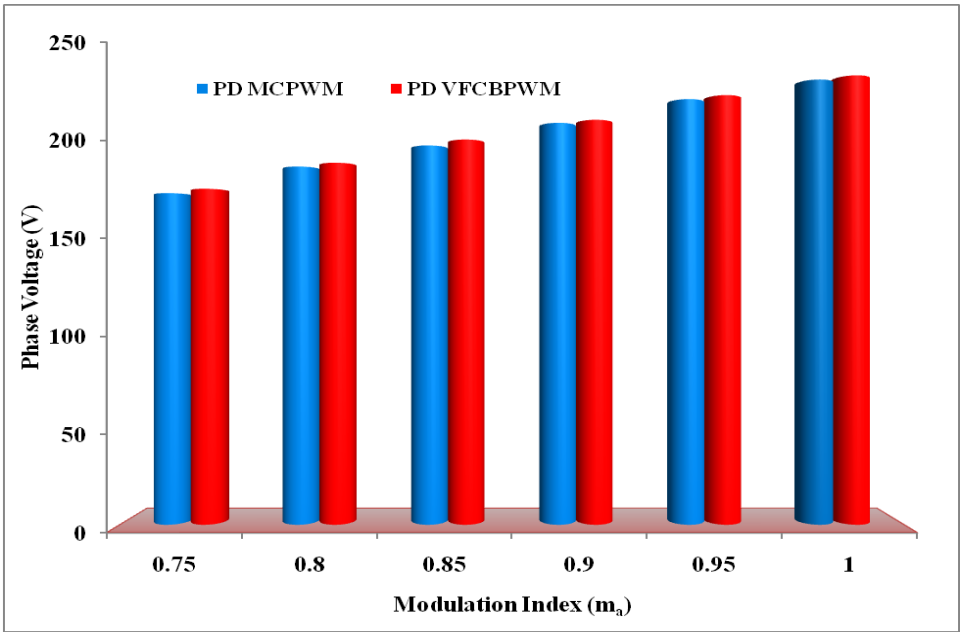

Figure 17 Modulation index Vs Phase voltage

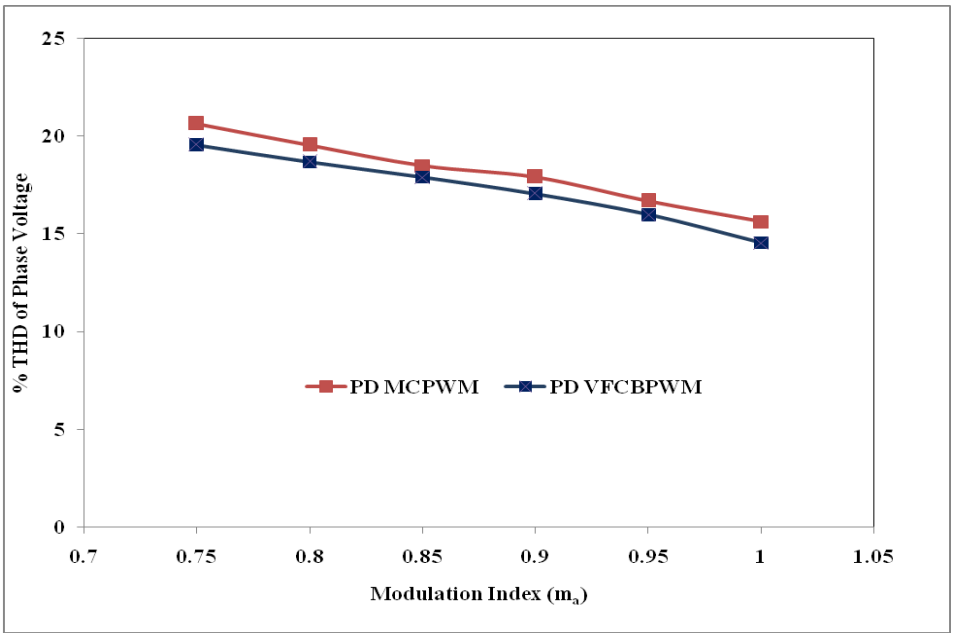

Figure 18 Modulation index Vs %THD of Phase voltage

Table 2 Performance comparison for the line voltage

Modulation Index (m_a)	Line Voltage (V)			
	MCPWM		VFCBPWM	
	V_{ab}	% THD	V_{ab}	% THD
1	408.5	12.97	415.1	11.44
0.95	388.7	13.90	394.2	12.27
0.9	367.5	15.06	372.9	13.54
0.85	348.8	16.22	353.7	14.60
0.8	326.6	17.64	331.3	15.21
0.75	306.4	18.33	312.6	16.29

EXPERIMENTAL RESULTS

The procedure extends to construct the new three phase SPSWCMLI with Insulated gate bipolar transistor power devices (IRG4BC20UPBF – Unidirectional device, FIO 50-12BD-Bidirectional device) and dc voltage sources of identical ratings used in simulation. The photograph in Fig.19 shows the experimental prototype used for examining the performance of the proposed MLI and the VFCBPWM strategy.

Figure 19 Experimental prototype

A field programmable gate array originates from an integrated circuit and can be configured to suit specific applications. It contains an array of reprogrammable logic blocks and a hierarchy of reconfigurable interconnects that allow the blocks to be wired together. The most common FPGA architecture consists of multiple I/O pads and routing channels of the same width. The flow diagram in Fig.20 describes the generation of pulse pattern in accordance with the VFCBPWM methodology.

The Figs.21 to 23 displays the switching pulses obtained using the theory of the VFCBPWM modulating mechanism from the Xilinx Spartan XC3SD1800A-FG676-4 Spartan 3A DSP FPGA board for the IGBTs.

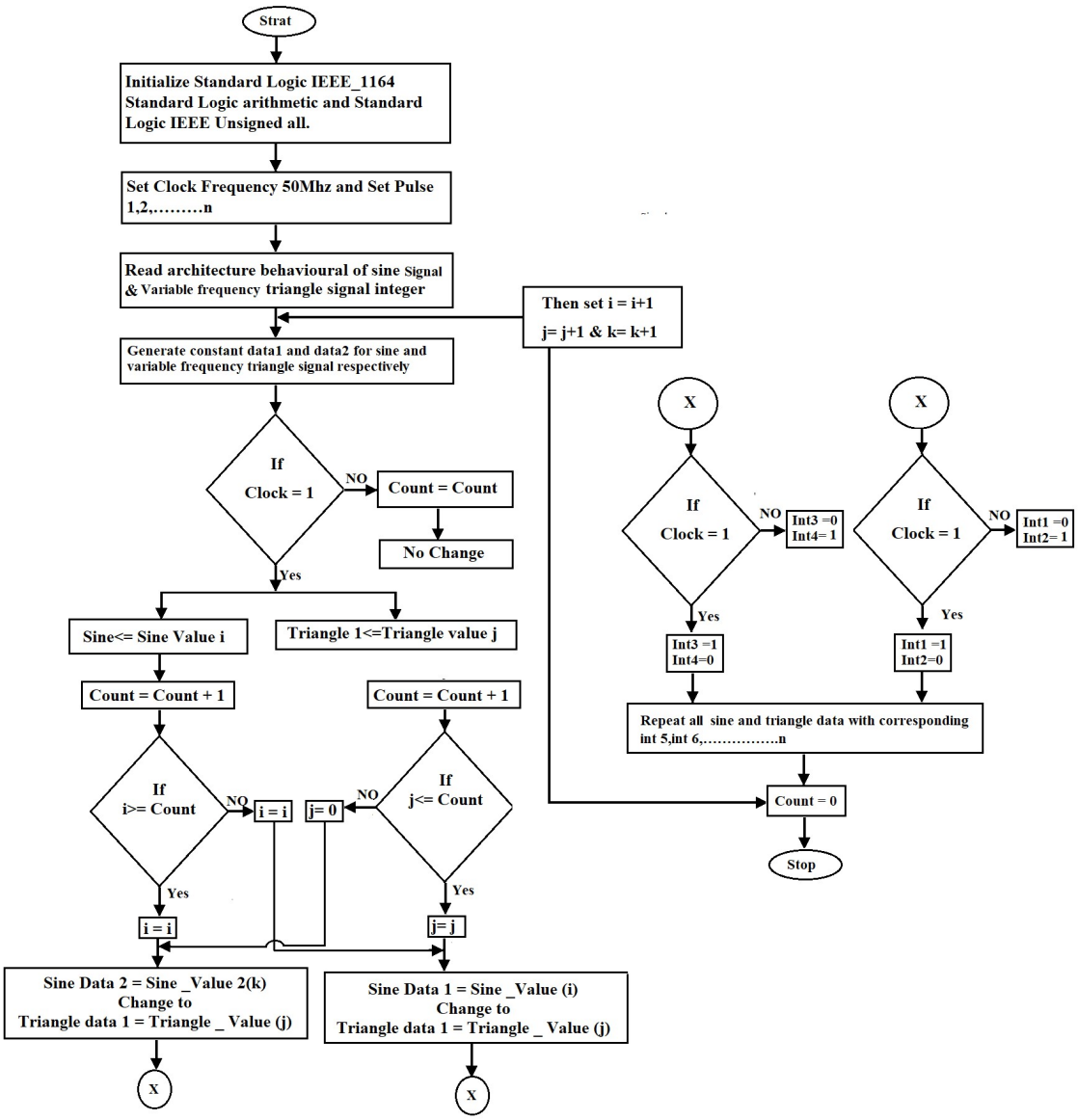

Figure 20 Flow diagram for generation of PD VFCBPWM Switching pulses

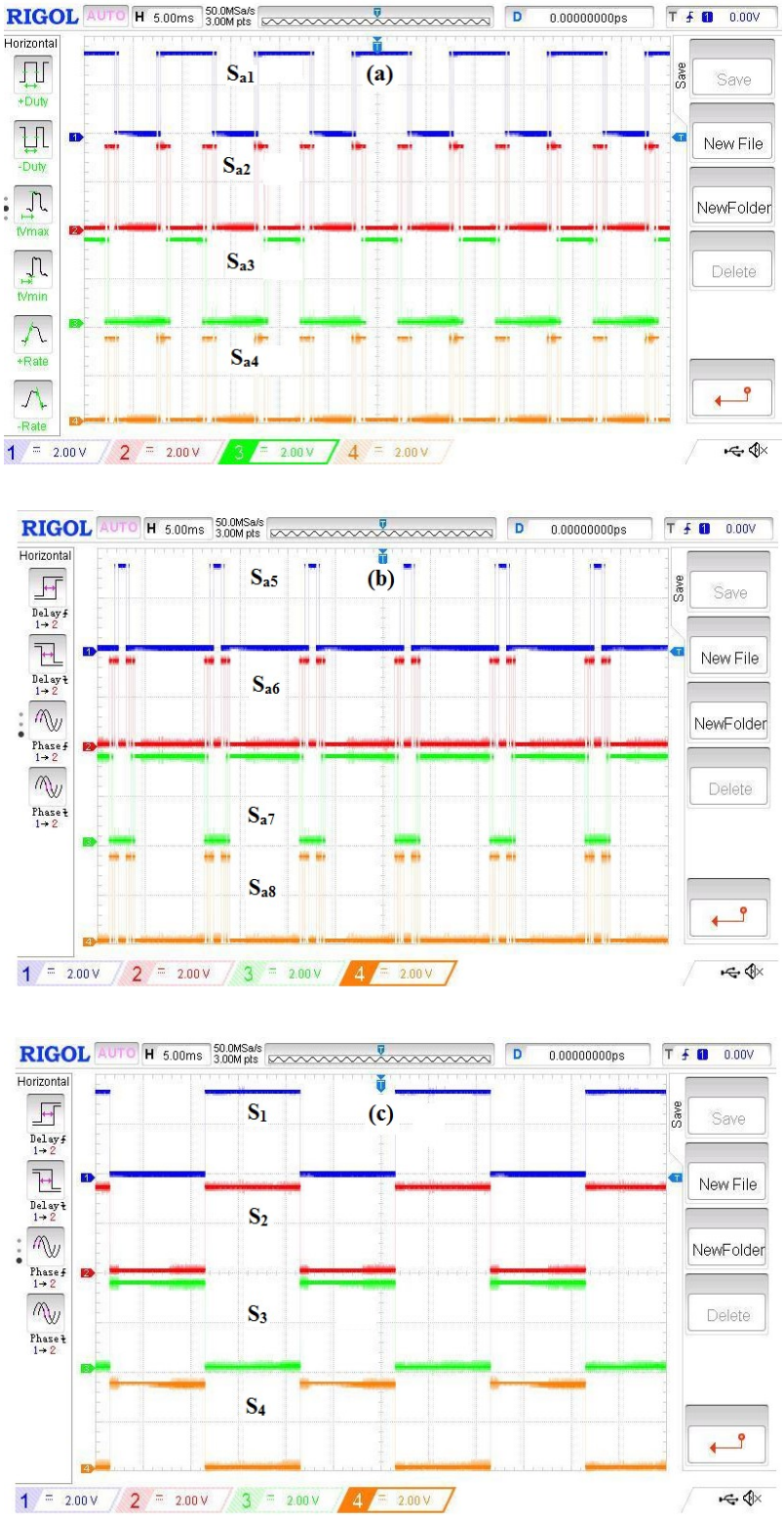

Figure 21 VFCBPWM Switching pulses for phase A (a) Cell 1 (b) Cell 2 (c) H-Bridge

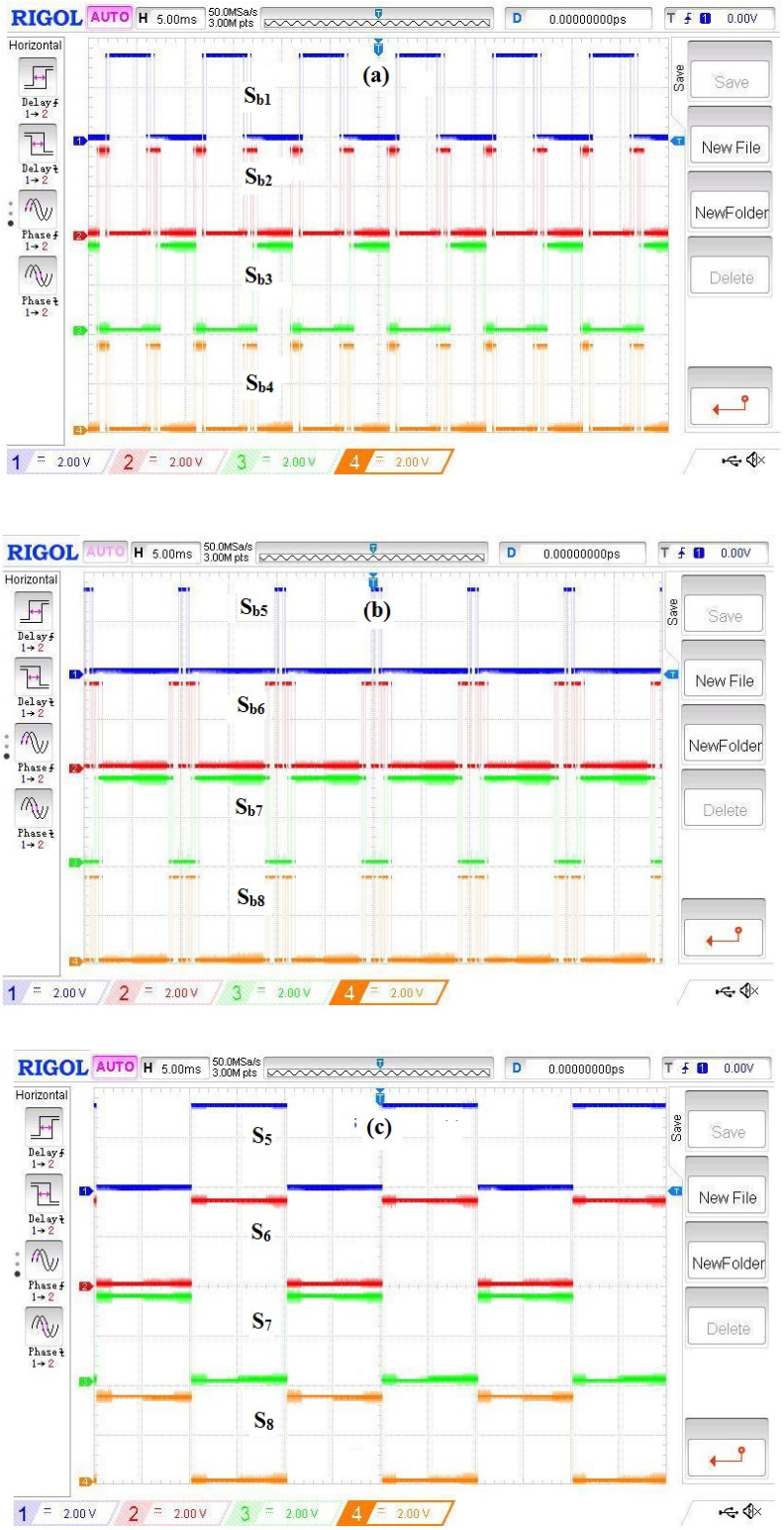

Figure 22 VFCBPWM Switching pulses for phase B (a) Cell 1 (b) Cell 2 (c) H-Bridge

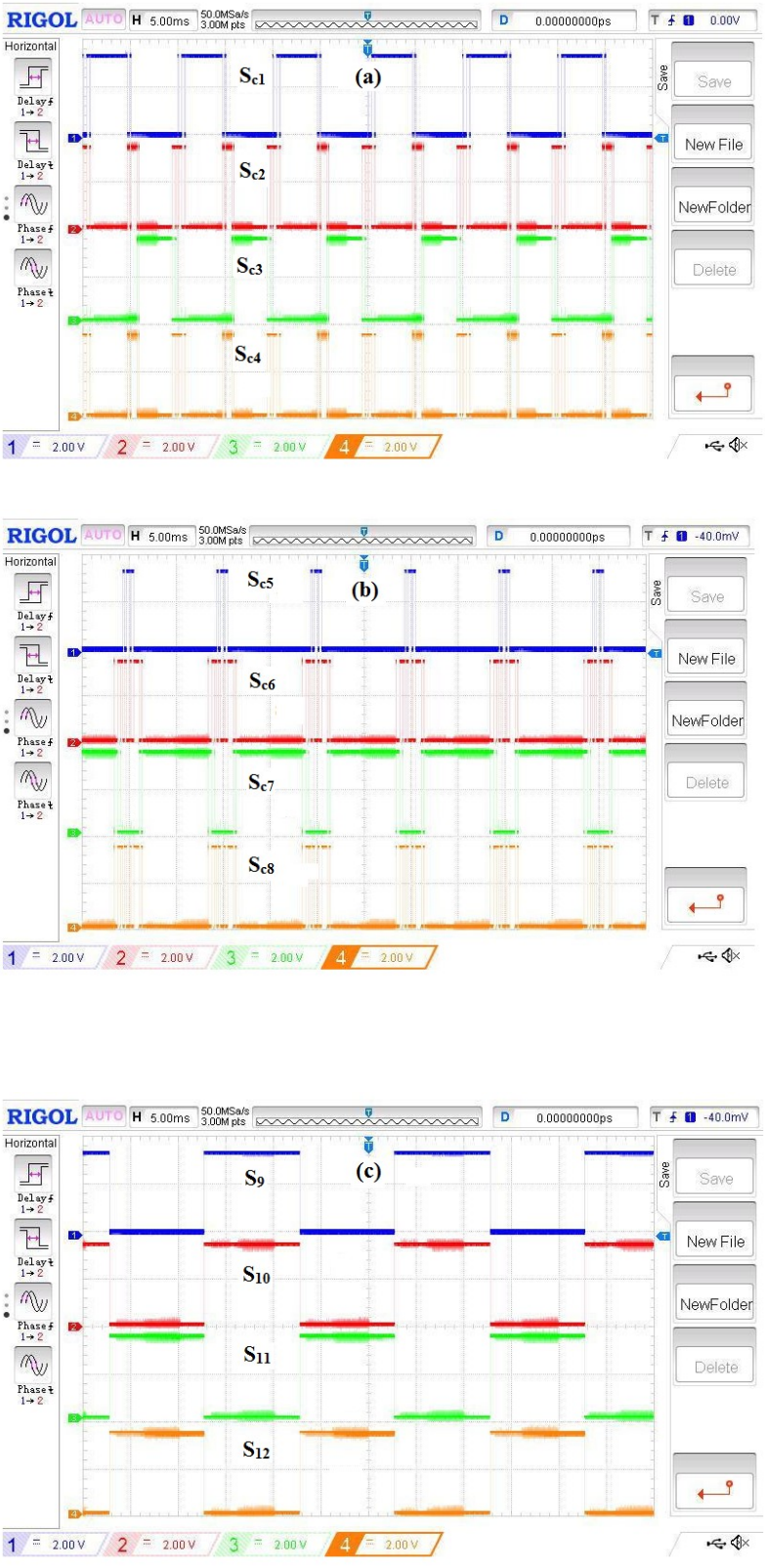

Figure 23 VFCBPWM Switching pulses for phase C (a) Cell 1 (b) Cell 2 (c) H-Bridge

The hardware results validate the simulated performance and the lower THD values for the VFCBPWM formulation seen through their respective voltage harmonic spectra in Figs.24 and 28. Table 3 compares the simulation and hardware results for VFCBPWM methodology.

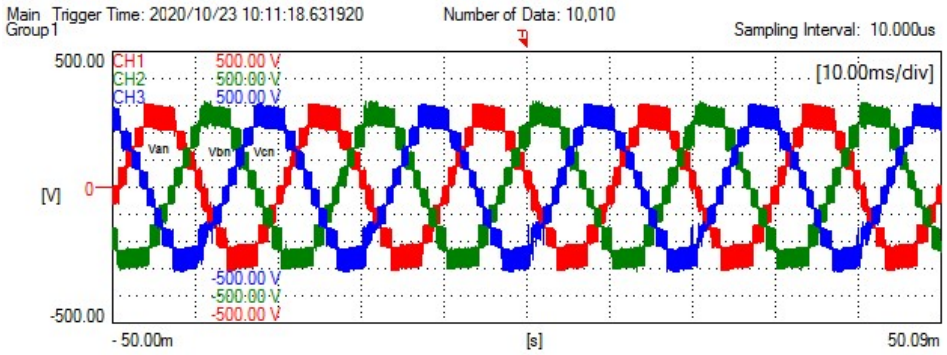

Figure 24 Phase voltage waveform for PD MCPWM

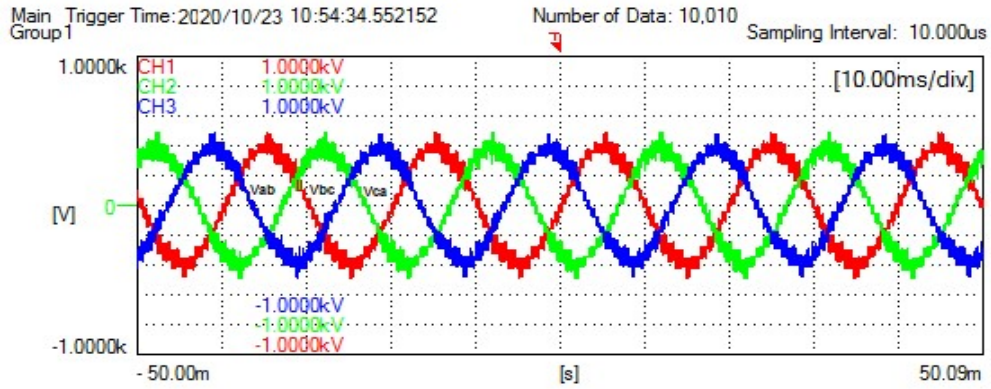

Figure 25 Line voltage waveform for PD VFCBPWM

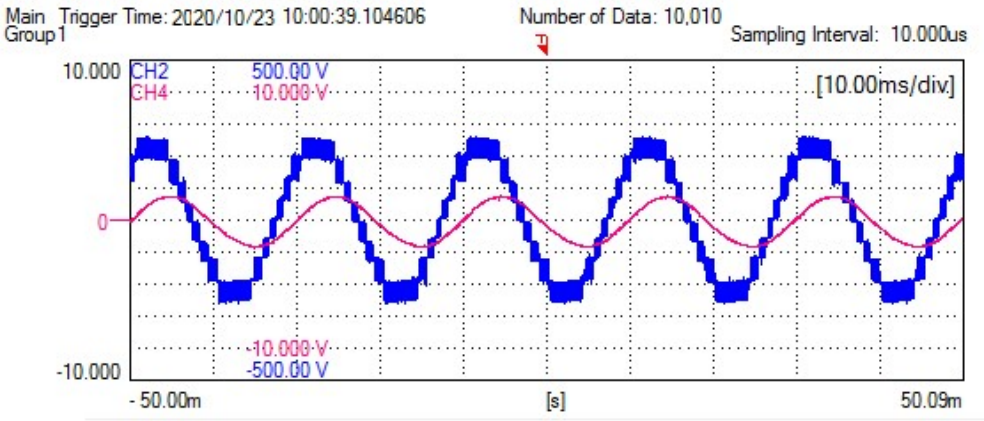

Figure 26 Phase voltage (Va) and current (Ia) waveform for VFCBPWM

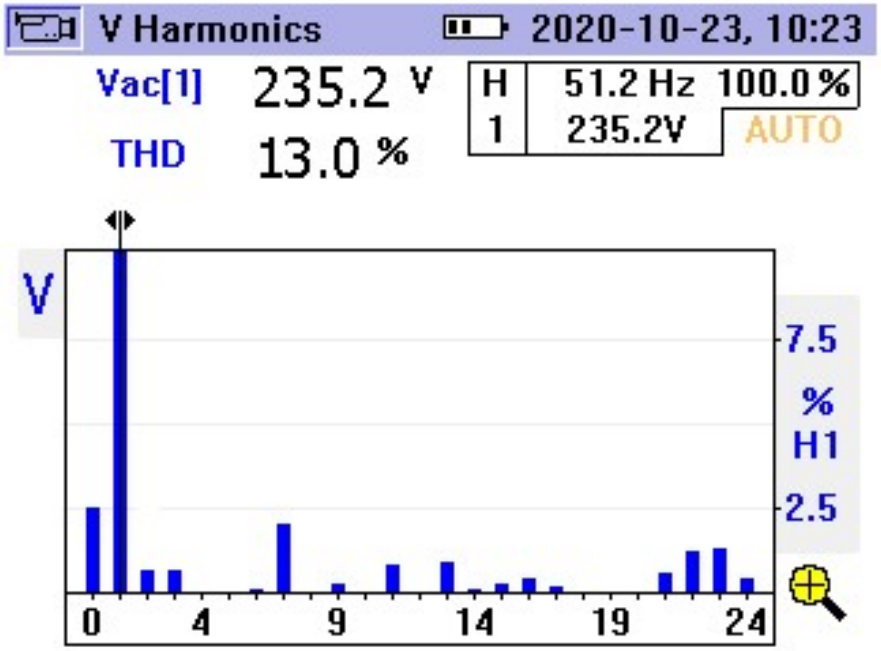

Figure 27 Phase voltage spectrum (V_a) for VFCBPWM

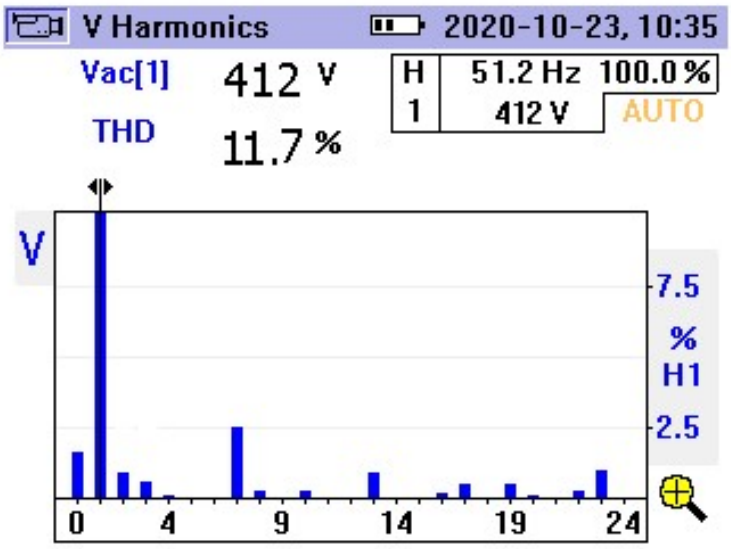

Figure 28 Line voltage spectrum (V_{ab}) for VFCBPWM

Table 3 Comparison of the line voltage

Modulation Index (m_a)	VFCBPWM Line Voltage (V)			
	Hardware		Simulation	
	V_{ab}	% THD	V_{ab}	% THD
1	412.0	11.70	415.1	11.44
0.95	391.7	12.95	394.2	12.07
0.9	369.2	13.88	372.9	13.14
0.85	351.3	14.76	353.7	14.20
0.8	329.1	15.87	331.3	15.11
0.75	310.2	16.74	312.6	16.19

CONCLUSION

The philosophy of VFCBPWM scheme was sought to balance the device switching's for all the levels of the SPSWCMLI. The methodology was cast to modulate the variable frequency carrier and the sinusoidal reference to produce a variable voltage. It was developed

to facilitate an increase in the fundamental component and consequently minimize the THD levels for both phase and line output voltages. The FPGA based experimental prototype was realized to establish the viability of the new SPSWCMLI topology and find a space in real world applications. The exquisite operation of the MLI will explore new areas of applications and carry the benefits of the formulation to reach industrial utilities. The comparative analysis was espoused to elucidate its merits over the MCPWM and project a new dimension for the use of the chosen MLI in various industrial applications.

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