DSP-Based Dual Converter – A Few Implementation Related Issues

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Abstract— In UG curriculum of Electrical Engineering, experiments on bi-directional DC drives, employing dual- converter, is often a part of the core UG curriculum. In such cases, custom-made dual converters, controlled by digital controllers and having the desired features and test points may be designed. This paper presents some of the important implementation-based issues, related to the fabrication of a laboratory-based dual- converter, operating in non-circulating-current-mode. The converter is controlled by a two-loop control-strategy, using the Digital Signal Controller dsPIC30F4011. Starting from the basics of dual-converter-operation, the paper gives an overall idea of the scheme and then takes up some of the implementation related issues in details. Exact schematics of actual set-up are presented, along with supporting experimental results, taken from the custom-made laboratory set-up.

Keywords— DC-drive; bi-directional control; dual converter; dsPIC30F4011; interfacing circuits; drivers; filters; SCR; dual-loop control

I. INTRODUCTION

SCR-based dual converters have been one of the classic topics of power-electronics and drives [1-2]. The topic has attracted wide research-interest over the decades [3-13]. While dual-converters have been utilized for different applications such as magnet power supplies [4], DC/DC converters as Inverse Dual Converter [5], cutting applications [6] etc., one of the widest application of this circuit is for achieving four- quadrant control of separately excited DC motors via armature voltage-control [7-12]. Due to the advances in AC drive technology, industrial application of dual-converter-based DC drives has receded over the years. However, academic interest in the subject still exists as it is a part of any UG curriculum on Electrical Engineering in India. Non-circulating current type SCR- based dual-converter (Fig. 1) forms one technique, by which bi-directional speed-control can be demonstrated in a laboratory. Although, such a technique has its own disadvantages like dead-zone and reduction of system gain and non-smooth behaviour during current-transfer [11], the technique also has some advantages like simplicity and low cost due to absence of the inter-phase reactor [11,13]. While a variety of control strategies, involving single [12] or multi- loop structures [9] may be used for such a laboratory set-up, the two-loop based control strategy, using an outer speed-loop and an inner current-loop are most commonly referred to. An outer slower speed loop, with a faster inner current loop, will achieve speed control, while maintaining the armature current within desirable limits [1,2,11]. While such converter-control can be achieved with analogue controllers [9,11], implementation of the lab-set-up using digital controller is advantageous in terms of cost and space-savings. In addition, such a set-up will add flexibility of testing various control strategies by altering the controller-firmware, or optimizing a given control-strategy by changing the parameter-values via firmware. Such implementations, using microprocessors [4,6,11] or digital signal processors [12] have already been attempted. However, keeping all the advantages of such a digital-controller based implementation in mind, it must be admitted that there are issues, which demands careful considerations, while implementing such digital-controller based set-ups in hardware. This paper addresses a few such issues, related to such a fabrication, involving an outer speed-loop and an inner current-loop, based on a single digital signal controller dsPIC30F4011. Some of the hardware issues, such as pulse- timing, feedback signal conditioning and driver-design, are addressed, along with the algorithm for control, in details. This paper is divided into five sections. Section-II presents the theory of a non-circulating current type dual-converter in brief. Section III takes up the implementation issues, such as selection of controller, power-devices and driver-design to make the set-up work successfully. It also addresses related issues, such as feedback signal processing and correct pulse delivery to ensure successful triggering

of SCRs over a wide- range of load and firing angles. Handy design equations are presented along with exact schematics of some of the circuits, related to the above. Section-IV presents some of the experimental results, taken from the fabricated laboratory set- up for dual-converter. Section-V presents the conclusions.

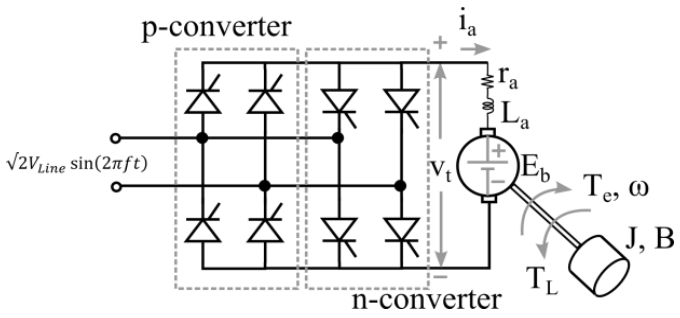

Fig. 1. Basic schematic diagram of a non-circulating-current type dual converter

I.DSP-Based Dual Converter: Principles

A dual converter consists of two controlled rectifiers, connected in anti-parallel mode across the armature of a DC motor. Such an arrangement can be used for bi-directional speed control of the connected DC motor, by armature-voltage control principle [1,2,8-11]. A simplified schematic-diagram, showing the non-circulating version of the above scheme is presented in Fig. 1. The basic governing equations, pertaining to the dynamic performance of such a system, in any direction, may be presented as follows:

$$\langle v_t \rangle = V_t = 0.9V_{Line}\cos\alpha \quad \text{.....(1)}$$

$$v_t - E_b = v_t - k\omega = r_a i_a + L\frac{di_a}{dt} \quad \text{.....(2)}$$

$$T_e - T_L = ki_a - T_L = J\frac{d\omega}{dt} + B\omega \quad \text{.....(3)}$$

Usually, dual-converter is used for closed-loop speed-control of the connected DC motor. Under such a case, the closed loop feedback scheme may be represented in Fig. 2, and the overall transfer function between the reference-speed-input and the actual output speed may be represented as follows:

$$G_{CL}(s) = \frac{G_1(s)G_{2CL}(s)}{1+G_1(s)G_{2CL}(s)} \quad \text{.....(4)}$$

The inner-current loop has a faster dynamic response than the outer-speed loop. Care is taken to ensure that the time- constants of the loops are matched, so as to ensure that the reference speed is successfully tracked, while ensuring that the armature-current does not remain above a set limit beyond a particular time-interval. In the following paragraphs, a few implementation-based issues, regarding a dual-converter- driven DC drive, controlled by a DSP-based controller-card using the two-loop control-scheme of Fig. 2, will be addressed.

II. Implementation Issues

A.Selection of Power Devices and Driver Design

The first step in the implementation of the hardware set-up is the selection of power devices for the dual converter,

under consideration. To determine the ratings of the power converter, it is essential to know the armature ratings of the DC motor, to be driven by the dual converter. For the experimental set-up, the motor used had the armature-circuit ratings of 220 V, 6 A.

Assuming that the motor will draw a nearly ripple-free DC current at full-load condition, and taking into account a safety factor of nearly 1.5 for current rating, the minimum average current rating of the SCR required should be around 9 A. Hence, the popularly available SCR model 16TTS12, which is

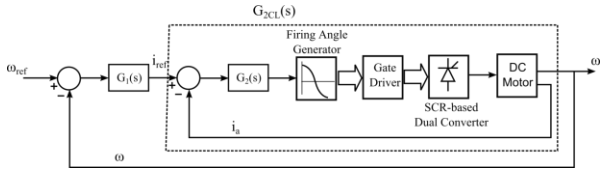

Fig. 2. A simplified block diagram for closed-loop speed control of a DC motor via dual-converter

having an average current rating of around 10 A and a voltage rating of up to 1600 V, is selected for the dual converter.

The driver circuit for the SCRs can be designed as per guidelines given in available literature. However, as the drivers will be fed with pulses from a DSP or some CMOS IC (low sourcing capability), a Darlington arrangement at the input-side of the driver may be opted for to reduce the loading effect on the logic ICs. The schematic diagram for such a driver circuit is shown in Fig. 3. The various steps in designing the main and auxiliary transistors for the driver are presented below.

Step-I: The main transistor is connected to the primary winding of the pulse-transformer (magnetizing inductance L_m). Its voltage and current ratings may be given by (5) and (6).

$$I_T = \frac{8}{L_m f_{sw}} \quad \text{.....(5)}$$

$$V_T = 24\left(1+\frac{R_{dschg}}{3L_m f_{sw}}\right) \quad \text{.....(6)}$$

Step-II: In case of the auxiliary transistor, which drives the main transistor, the voltage rating should be at least 24 V (i.e. 20% over the rated value of 20 V), while its current rating is given by:

$$I_{T,aux} = \frac{I_T}{\beta_1} \quad \text{.....(7)}$$

The value of β_1 and β_2 may be taken as 10. The values of the resistors may be computed R_4 and R_5 may be computed as follows:

$$R_4 = \frac{24}{I_{T,aux}} \quad \text{.....(8)}$$

Assuming R_5 to be a small resistance (a few ohms), the value of the base resistance R_6 may now be computed as follows:

$$R_6 = \frac{\beta_1\beta_2 V_{pulse}}{I_T} - \beta_2 R_5 \quad \text{.....(9)}$$

Step-III: A small resistance may be connected in series with the primary of the pulse transformer to protect the transistor and transformer from over-current due to accidental core- saturation. Its value may be computed as follows:

$$R_1 = \frac{24}{I_T} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (10)$$

B.Selection of Controller

SCR-based dual converter control can be achieved by analogue controllers. However, here the main aim is to implement the control via a digital controller. Many digital controllers, having the minimum required memory, speed and terminal pins can be used for this application. However, to maintain flexibility in programming and also to test the performance of a state-of-the-art digital controller for the above application, a 16-bit microcontroller with an in-built DSP engine, namely dsPIC30F4011 [14], has been used for the above application. It has many powerful peripheral- modules, out of which, two peripherals, namely the PWM port and the ADC port has been used for this application. The ADC module has ten different input pins to scan and digitize ten different input analogue signals. Here, three such pins have been used for feeding in (a) the speed-reference signal, (b) the

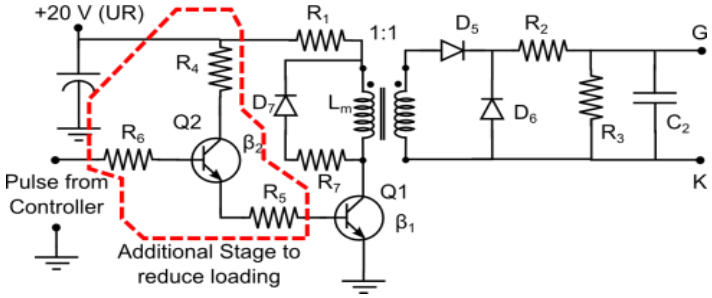

Fig. 3. Schematic diagram of the driver circuit for one SCR

speed-feedback signal and (c) the armature current signal. In addition, a direction input (forward or reverse) has also been fed through a separate pin. The PWM port has eight PWM pins, which can be programmed for a variety of power- electronic applications. Four such PWM pins have been used for controlling the eight different SCRs for the dual converter. Fig. 4 presents the schematic of the controller card, based on the above digital controller. Note that to avoid loading on the PWM pins, the output pulses have been transmitted through buffers.

C.Interfacing for Feedback Control

As shown in Fig. 2, two feedback-signals are required for implementing the dual-loop control-scheme. The outer loop, involving speed-feedback is the slower one, operated by a P-I controller. The inner loop is based on armature-current feedback and is operated by an adaptive hysteresis controller. For a motor, running on no-load or light load, the armature current is far from constant, but has plenty of ripples of twice the supply frequency f_s Hz over some DC

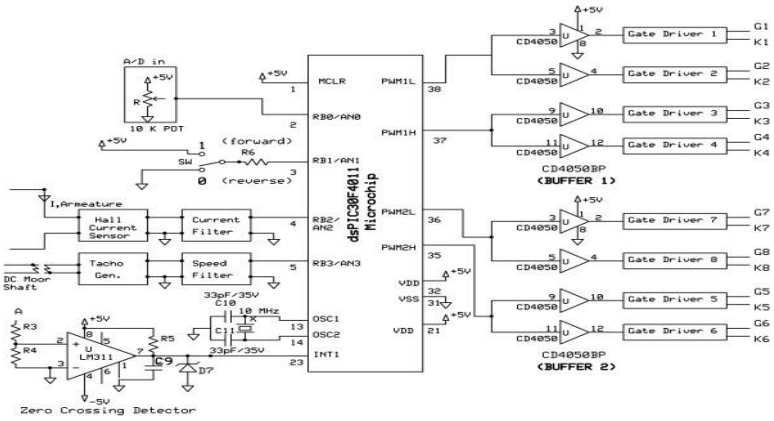

Fig. 4. The schematic of the controller card used for the dual-converter control application

component. To make the control-scheme work properly, the current must be sensed accurately with linearity and isolation. A suitable Hall- Effect Sensor may be used for this purpose. The Hall-Effect transducer HY-25P has been used for this set-up. Secondly, only the DC component of the current should reach the controller, with the value not

exceeding 5 V (the supply voltage of the DSP). Hence, it is essential to design a low-pass filter to properly filter out the ripples and transmit only the DC component to the controller. A low-pass second order Butterworth-Filter, shown in Fig. 5, is selected for this purpose, since it gives a flat-flat-response. The basic design equations for the low-pass Butterworth filter are presented here, with respect to Fig. 5, for easy reference. These equations can be used directly to design such a filter.

Step-I: The cut off frequency of this filter is set at 1/20 of the supply frequency, resulting in the equation:

$$R_1 C_1 = \frac{10}{\pi f_s} \qquad \text{----------(11)}$$

Choosing a standard value of C1 (AC capacitor), the value of R1 can be calculated.
Step-II: The value of *Rf* and *R2* may be calculated by choosing some standard value for *R2* and then selecting *Rf* by using the following equation:

$$\frac{R_f}{R_2} = 0.586 \qquad \text{----------(12)}$$

Step-III: Finally, a potential divider may be placed at the output of the filter so as to make the DC gain of the filter to be unity. The basis of designing this potential-divider network is presented in the following equation:

$$\frac{R_4}{R_3 + R_4} = 0.6305 \qquad \text{----------(13)}$$

As the motor-inertia contributes to make the speed signal from the tacho-generator to be “filtered”, a second order Butterworth filter may not be needed in this case. However, the designer may re-use (11) – (13) to design a first order Butterworth Filter to suit the application (Fig. 5). Protective Zener diodes (4.7 V, 0.5 W) may be used at the output of each filter to ensure that the voltage remains clamped below 5 V. Suitable scaling by potential-divider circuit may be implemented at critical points to (a) maintain linearity and (b) ensure that eventually the voltage reaching the DSP pin is below 5 V.
With the properly “conditioned” feedback signals, the controller will work satisfactorily, if correct triggering is achieved at all loads. Usually, at heavy loads (continuous load current with minimal ripple), triggering can be achieved at any firing angle. However, at low and light loads, due to the presence of back-EMF from the motor-armature, a particular triggering angle may not be suitable for turning on the SCR, since it is already reverse-biased due to the back-EMF (Fig. 6). Hence to avoid such issues, the following actions are taken, within the firmware of the controller:
• It is ensured that multiple pulses are transmitted for each

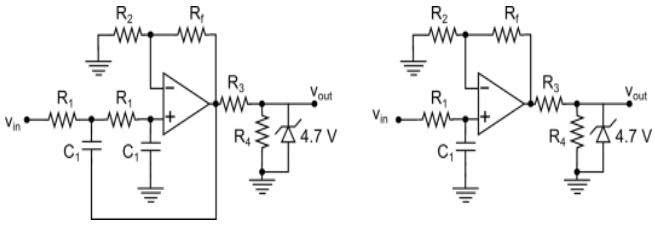

Fig. 5. Second order low pass filter for armature current (left) and 1st order low pass filter for speed (right)

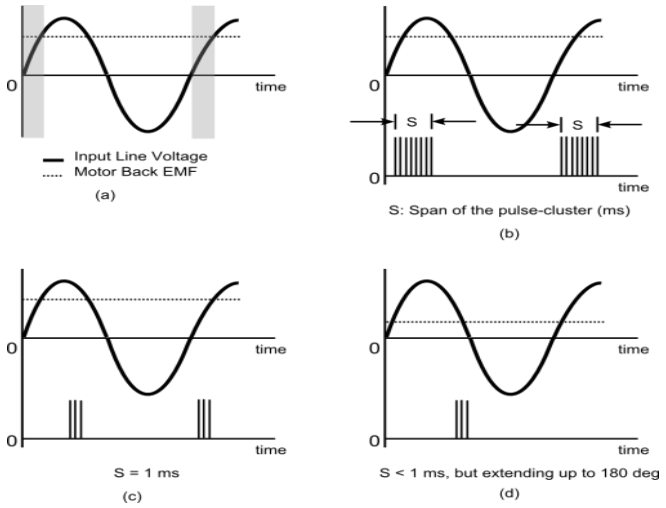

Fig. 6. (a) Grey zones showing the regions, where triggering cannot be achieved; (b) firing angle less than 90^o and pulse-cluster extending up to 90^o; (c) firing angle greater than 90^o and pulse-cluster having a span of 1 ms and (d) pulse cluster extending up to 180^o, but having a span less than 1 ms

triggering. Such pulse-cluster may span for around 1 ms.

- For all firing angles less than 90^0, it is ensured that the pulse-cluster is extended till 90^0 or for 1 ms, whichever is more.
- For all firing pulses beyond 90^0, the pulse-cluster is maintained for 1 ms, or up to 180^0, whichever is less.

The above are illustrated in Fig. 6.

D.Implementation of the Overall Control Logic via Firmware

The overall control-logic for the dual converter, as per the dual-loop control structure (Fig. 2) has been implemented on the single DSP. The block diagram of the complete system is presented in Fig. 7. The control-algorithm, as implemented via firmware within the DSP may be summarized as below:

1. Initialize all necessary modules. Run start-up checks.
2. Read the direction command status (forward or reverse); store the same in memory.
3. Identify the SCRs to be triggered.

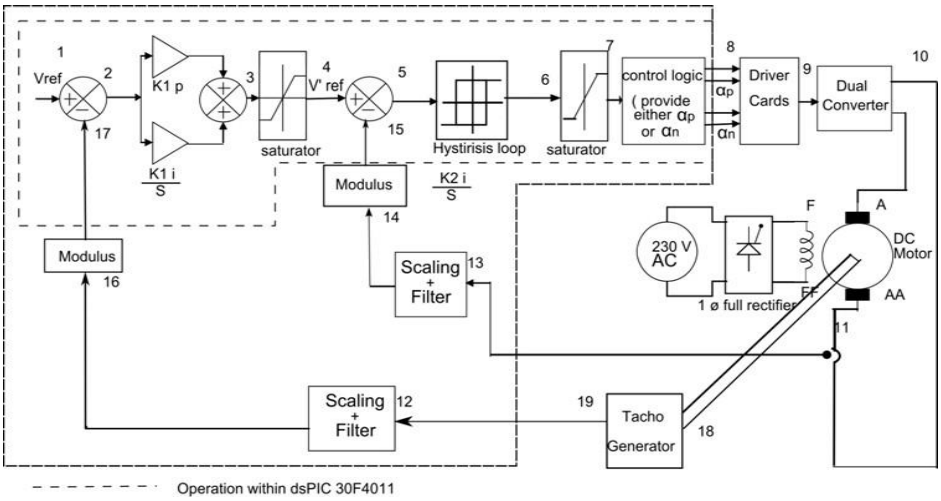

Fig. 7. Overall block diagram of the system after implementation of the logic within the DSP via firmware

4. Read the speed input and speed feedback signals and compute the error and amplify the same through the P-I controller.
5. Read the current feedback and compare the same with the P-I controller output (acting as current-reference) to compute the digital hysteresis controller output, which will adjust the firing angle in steps.
6. Set the "computation-over flag" and wait till "computation- over flag" is cleared again.
7. Once the Zero-Crossing of the line voltage generates the interrupt, go to the interrupt service routine (ISR), generate the appropriate delay (as governed by the computed firing angle) and clear the "computation-over flag".
8. Read the status flag (forward or reverse) and compare it with the saved status value. If different from the saved status value, then save this new value in the memory and identify the SCRs to be triggered. Gradually increase the firing angle of the outgoing converter to 180°, stop pulses to all SCRs for around 2 sec, and then trigger the SCRs of the incoming converter at a firing angle of just less than 180° and then gradually reduce the firing angle to reach the original value.
9. Go to step no. 4.

IV. Results from the Experimental Set-up

The above logic was implemented via a C30 program, written in the MPLAB environment and loaded on to the controller via the ICSP programmer. Upon successful implementation of the hardware circuit and the allied firmware, the set up gave acceptable results, some of which are presented in this section in Figs. 8 - 12. A photograph of the fabricated laboratory set-up is shown in Fig. 13.

V. Conclusion

Some implementation based issues, related to the fabrication of a laboratory set-up for a DSP-controlled dual-converter fed DC motor drive is discussed in this paper. Issues such as the use of Darlington-pair transistors for the drivers, correct pulse-cluster-span for various firing angles to ensure successful triggering under various loading conditions, use of correctly designed filters for current and speed feedback signals and scaling and amplification thereof have been presented. Some of the experimental results from the fabricated laboratory set-up have also been added to show that the implemented hardware and firmware are working correctly.

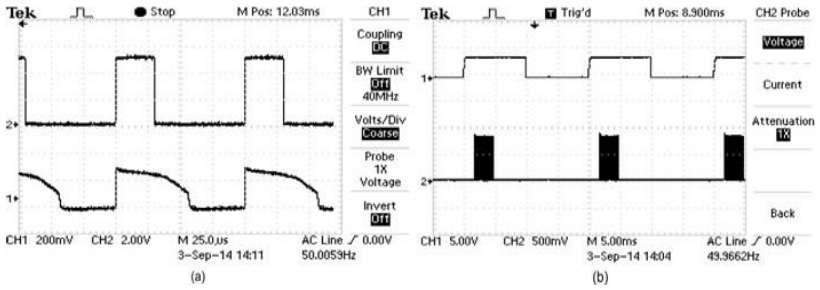

Fig. 8. (a) Individual triggering pulses at the pin of the DSP (top) and at the gate-cathode terminal (bottom); (b) Output of the zero- crossing-detector for the input line voltage (top) and pulse-cluster for a triggering angle of around 20 degree (bottom)

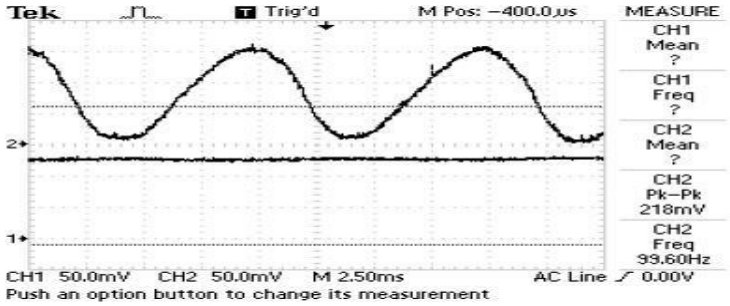

Fig. 9. Actual armature current (top) and filtered and amplified version after passing through the low pass Butterworth Filter (bottom); Scale: Y-axis: 2 A/div (both channels), X-axis: 2.5 ms/div.

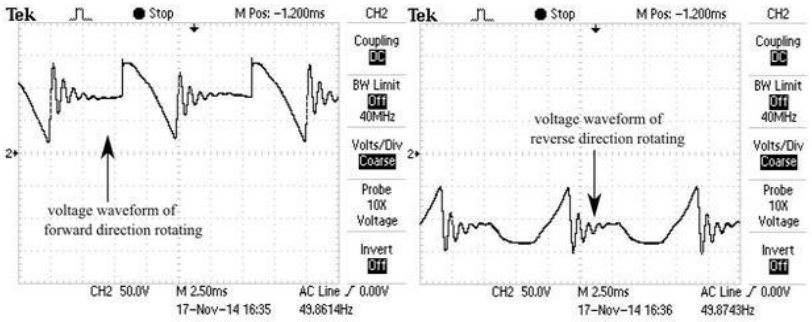

Fig. 10. Output voltage waveform of the dual converter on light load in forward direction (left) and reverse direction (right), illustrating successful SCR triggering

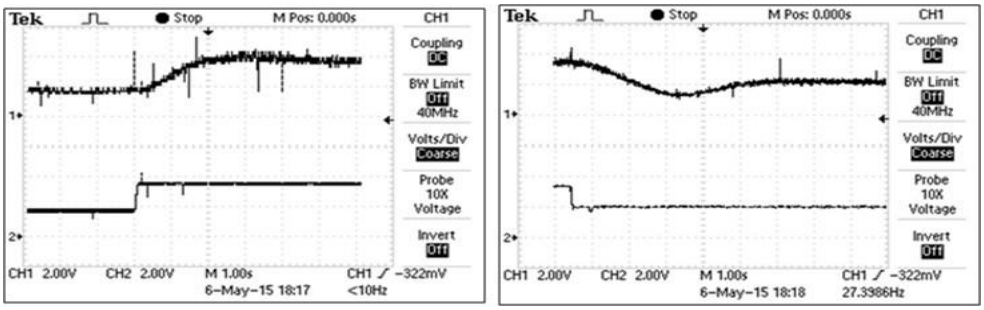

Fig. 11. Actual speed (top) following reference speed (bottom) for a step-increase (left) and for a step-decrease (right) in the reference signal

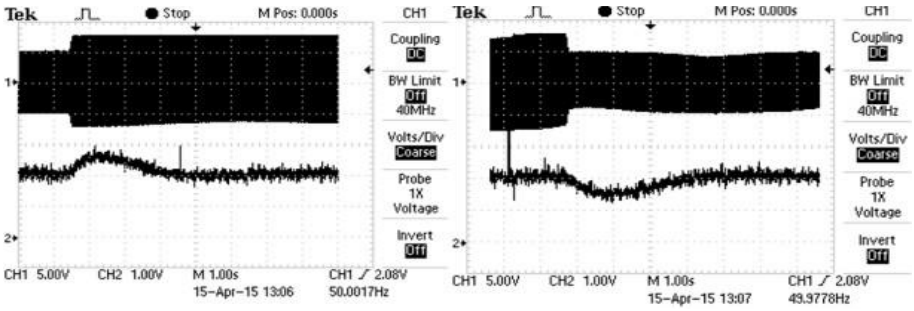

Fig. 12. Input voltage envelope experiencing a sudden rise (left) and fall (right) (Y-axis: 200 V / div); Bottom: Speed of the motor first experiences a transient disturbance then comes back to the set value in both the cases (Y-axis: 500 rpm/div); X-axis: 1 sec / div (for both channels)

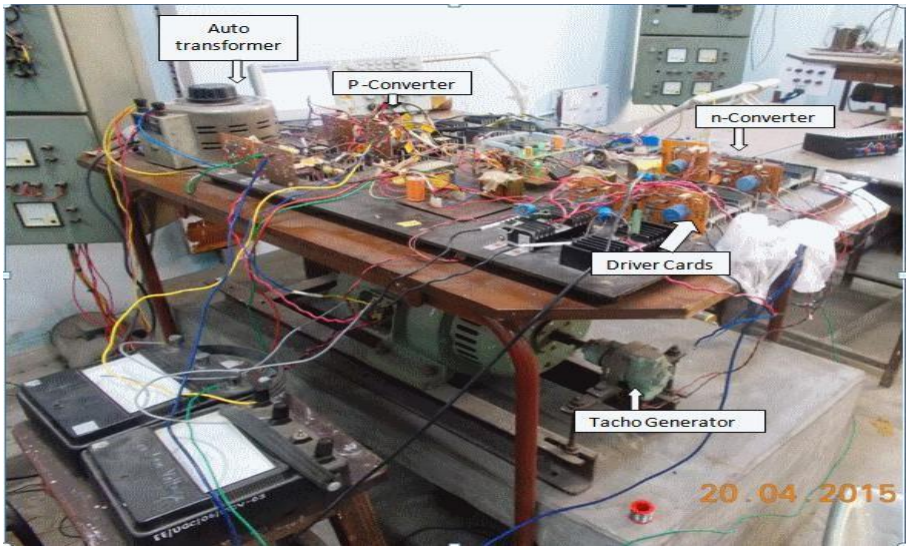

Fig. 13. A picture showing the various components of the experimental set-up

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