

Level Inverter

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Abstract - The rapid adoption of multi-level inverters in electric drives and renewable energy systems highlights their crucial role in modern power electronics. These inverters provide significant advantages over traditional two-level inverters, such as reduced dv/dt stress, lower total harmonic distortion (THD), and decreased common mode current. However, common multi-level inverter topologies, like neutral point clamped, cascaded H-bridge, and flying capacitor inverters, encounter challenges that hinder optimal performance. This paper introduces an innovative three-phase two-level inverter topology designed to address common mode voltage and current issues found in existing designs. The proposed topology combines two cascaded converters and uses device junction capacitance (DJC) to implement a neutral point clamping methodology, enhancing the inverter's stability and efficiency. A detailed analysis using the switching function concept demonstrates the impact of DJC on inverter performance. The study also presents an advanced PWM control scheme to optimize the modulation process and minimize common mode voltage variations. MATLAB simulation results show the proposed topology's superiority over conventional and H7 two-level inverters, with significant improvements in key performance metrics such as pole voltage, phase voltage, common mode voltage, and THD. The proposed inverter reduces THD to 61.41%, compared to 91.81% and 88.01% for conventional and H7 inverters, respectively.

This research not only advances the field of power electronics but also provides practical insights for engineers and researchers. By addressing critical issues in multi-level inverter design, the proposed topology paves the way for more efficient and reliable power conversion systems, contributing to enhanced energy efficiency and sustainability in contemporary applications.

Keywords— Multi-level inverters, three-phase inverters, common mode voltage, device junction capacitance (DJC), pulse width modulation (PWM), total harmonic distortion (THD), neutral point clamping.

Introduction

In contemporary applications, the importance of multi-level inverters is paramount, especially in electric drives and renewable energy systems. Their adoption is driven by advantages over traditional two-level inverters, including reduced dv/dt stress, lower total harmonic distortion (THD), and decreased common mode current. Despite their appeal, existing multi-level inverter topologies, such as neutral point clamped, cascaded H-bridge, and flying capacitor inverters, have their limitations.

The neutral point clamped multi-level inverter, though widely used, faces issues like neutral point fluctuations, compromising system stability and performance. The cascaded H-bridge multi-level inverter requires independent DC sources, adding complexity and cost. The flying capacitor multi-level inverter, while promising, struggles with charging flying capacitors, introducing operational and control complexities.

Given these limitations, there is a need for novel solutions that can overcome these challenges while leveraging the advantages of multi-level inverters. This paper proposes a new three-phase two-level inverter topology designed to address common mode voltage and current issues. Building on prior research and insights from existing topologies, our novel approach aims to balance performance, efficiency, and complexity.

The primary goal of this study is to explore the proposed topology comprehensively, elucidating its performance characteristics and potential applications across various scenarios. Through rigorous analysis and simulation, we aim to demonstrate the efficacy of our design in mitigating common mode voltage and current while maintaining system efficiency and reliability.

Furthermore, our investigation extends to examining the impact of the proposed topology on electromagnetic compatibility, a crucial aspect in modern power electronics systems. Addressing these aspects is vital for ensuring seamless integration and operation of multi-level inverters in real-world applications.

In conclusion, this research not only advances power electronics but also serves as a practical guide for engineers and researchers in the field of multi-level inverter design. As the demand for efficient and reliable power conversion systems increases, innovative solutions like the one proposed here are key to enhancing energy efficiency and sustainability.

I. PROPOSED TOPOLOGY OF THE THREE-PHASE TWO-LEVEL CMLI

The circuit of the proposed three phase two level CMLI is shown in Fig.1

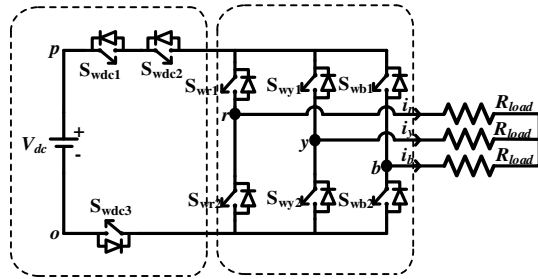


Fig.1 Circuit diagram of the proposed three-phase two-level CMLI

The circuit schematic of the proposed three-phase three-level inverter connected to a resistive load is shown in Fig. 1. The DC voltage source having a magnitude of ' V_{dc} ' is connected to Converter '1' between the input terminals ' p ' and ' o ' of the three-phase three-level inverter. The proposed three-level inverter consists of a two-level inverter and three freewheeling switches S_{wdc1} , S_{wdc2} , and S_{wdc3} . The three-phase output terminals ' r ', ' y ' and ' b ' of the three-phase three-level inverter are connected to the resistive load ' R_{load} '.

The topology consists of two cascaded converters, viz. *Converter 1* and *Converter 2*. *Converter 1* consists of 3 switches – S_{wdc1} , S_{wdc2} and S_{wdc3} . This converter aids in neutral point clamping during the common zero states. *Converter 2* is a regular three phase bridge inverter circuit, composed by the six switches, S_{wr1} , S_{wr2} , S_{wy1} , S_{wy2} , S_{wb1} and S_{wb2} . A dc voltage V_{dc} is connected to the input side of *Converter 1*. The output terminals r , y and b of the inverter are connected to resistive load. The currents flowing through phases r , y and b have been represented as i_r , i_y and i_b , respectively.

The most notable feature of this inverter circuit is the usage of device junction capacitance in converter 1 and converter 2 to implement neutral point clamping methodology for the reduction of common mode voltage. Freewheeling in converter 2 is taken care. During normal operation of inverter converter '1' is freewheeling i.e., when switch S_{wx12} , where $x = 'r', 'y', 'b'$ are under operation. Converter '2' is in freewheeling i.e., when switch S_{wx12} , where $x = 'r', 'y', 'b'$ are in on state, when converter '1' is under operation.

The three-phase two-level inverter normally generates two levels ' V_{dc} ' and ' 0 ' in the pole voltage. Whenever any of the upper switch ' S_{wx1} ' where ' $x = 'r', 'y'$ ' and ' b ' in the three-phase two-level inverter are turned ON, then a pole voltage ' V_{dc} ' will be generated in the corresponding pole voltage as shown in Fig. 2(i). Similarly, whenever any of the lower switch ' S_{wx2} ' in the three-phase two-level inverter is turned ON, then a pole voltage ' 0 ' will be generated in the corresponding pole voltage as shown in Fig. 2. (ii) The DJC [9] is the capacitance across the power semiconductor switch. In the case of MOSFET, the DJC will be across the drain and source whereas for the IGBT the DJC will be across the emitter and collector. The

circuit schematic of three-phase two-level inverter by incorporating the DJC is shown in Fig. 3(a).

III. Analysis of two-level inverter using switching function concept including the effect of DJC

For analyzing the effect of DJC on the two-level inverter, the switching function concept is used. Fig. 3 shows the circuit of a two-level inverter with the switching function incorporated DJC. Whenever, the switch ' S_{wxk} ' where ' $x = 'r', 'y'$ ' and ' b ' and ' $k = '1'$ ' and ' 2 ' is turned ON, then the switching function ' S_{xk} ' for the corresponding switch will be equal to ' 1 '. As a result, the magnitude of the impedance across the switch will be equal to zero and the effect of DJC across the switch will be neglected. Whenever, the switch ' S_{wxk} ' is turned OFF, then the switching function ' S_{xk} ' for the corresponding switch will be equal to ' 0 '. As a result, the magnitude of the impedance across the switch will be equal to ' $1/j\omega C$ ' due to the effect of DJC across the switch. In order to study the effect of DJC on the two-level inverter, the expressions for the pole voltages and phase voltage of the two-level inverter need to be obtained.

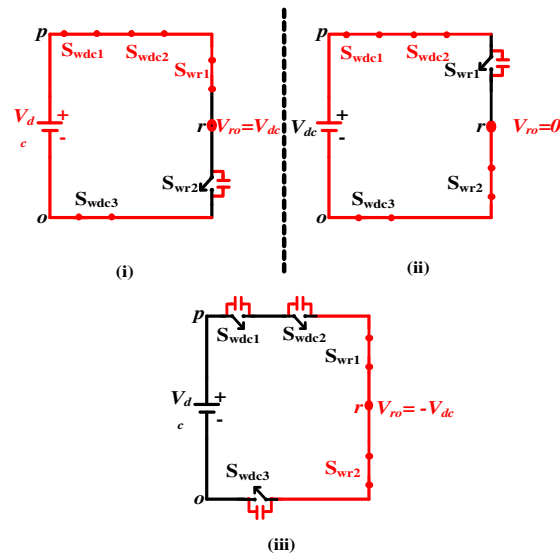


Fig.2 Circuit schematic of three-phase two-level inverter considering DJC.

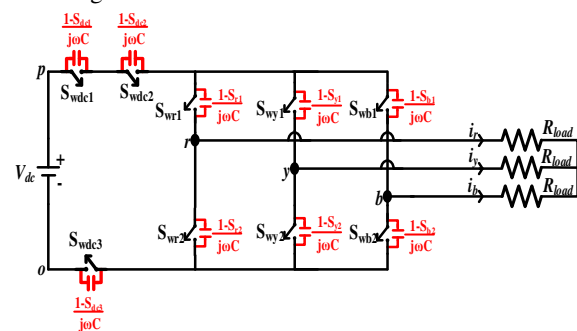


Fig. 3 Circuit schematic of three-phase two-level inverter by incorporating the DJC.

From Fig. 3, the expression for the pole voltages ' v_{ro} ', ' v_{yo} ' and ' v_{bo} ' are given by

$$V_{ro} = \frac{\frac{V_{dc} \times ((1-S_{r2}) + (1-S_3))}{j\omega_c}}{\frac{1}{j\omega_c} ((1-S_{r2}) + (1-S_{r1}) + (1-S_1) + (1-S_2) + (1-S_3))}$$

$$V_{ro} = \frac{V_{dc} \times ((1-S_{r2}) + (1-S_3))}{((1-S_{r2}) + (1-S_{r1}) + (1-S_1) + (1-S_2) + (1-S_3))}$$

Similarly for phase 'y' is given as:

$$V_{yo} = \frac{\frac{V_{dc} \times ((1-S_{y2}) + (1-S_3))}{j\omega_c}}{\frac{1}{j\omega_c} ((1-S_{y2}) + (1-S_{y1}) + (1-S_1) + (1-S_2) + (1-S_3))}$$

$$V_{yo} = \frac{V_{dc} \times ((1-S_{y2}) + (1-S_3))}{((1-S_{y2}) + (1-S_{y1}) + (1-S_1) + (1-S_2) + (1-S_3))}$$

Similarly for phase 'b' is given as:

$$V_{bo} = \frac{\frac{V_{dc} \times ((1-S_{b2}) + (1-S_3))}{j\omega_c}}{\frac{1}{j\omega_c} ((1-S_{b2}) + (1-S_{b1}) + (1-S_1) + (1-S_2) + (1-S_3))}$$

$$V_{bo} = \frac{V_{dc} \times ((1-S_{b2}) + (1-S_3))}{((1-S_{b2}) + (1-S_{b1}) + (1-S_1) + (1-S_2) + (1-S_3))}$$

For the ease of calculation let us consider $S_{r1}' = (1-S_{r1})$, $S_{r2}' = (1-S_{r2})$, $S_{y1}' = (1-S_{y1})$, $S_{y2}' = (1-S_{y2})$, $S_{b1}' = (1-S_{b1})$, $S_{b2}' = (1-S_{b2})$ and $S_{123}' = (1-S_1) + (1-S_2) + (1-S_3)$

Common mode voltage is given as:

$$V_{cm} = \frac{V_{ro} + V_{bo} + V_{yo}}{3}$$

$$V_{cm} = \frac{1}{3} \left[\frac{V_{dc} \times (S_{r2}' + (1-S_3))}{(S_{r1}' + S_{r2}' + (1-S_1) + (1-S_2) + (1-S_3))} + \frac{V_{dc} \times (S_{y2}' + (1-S_3))}{(S_{y1}' + S_{y2}' + (1-S_1) + (1-S_2) + (1-S_3))} + \frac{V_{dc} \times (S_{b2}' + (1-S_3))}{(S_{b1}' + S_{b2}' + (1-S_1) + (1-S_2) + (1-S_3))} \right]$$

The phase voltages ' v_{xn} ' can be obtained by subtracting the pole voltages ' v_{xo} ' and common mode voltage ' v_{cm} '

$$V_{ry} = \frac{\text{num1}}{(S_{r1}' + S_{r2}' + S_{123}') \times (S_{y1}' + S_{y2}' + S_{123}') \times (S_{b1}' + S_{b2}' + S_{123}')} \times V_{cm}$$

$$V_{yb} = \frac{\text{num2}}{(S_{y2}' + S_{y1}' + S_{123}') \times (S_{b2}' + S_{b1}' + S_{123}')} \times V_{cm}$$

$$V_{rb} = \frac{\text{num3}}{(S_{r2}' + S_{r1}' + S_{123}') \times (S_{b2}' + S_{b1}' + S_{123}')} \times V_{cm}$$

$$\text{num1} = V_{dc} \times \left[\begin{array}{l} (S_{r2}' + S_{y2}') \times (S_{y2}' + S_{y1}' + S_{123}') \\ - (S_{y2}' + S_{y1}') \times (S_{r2}' + S_{r1}' + S_{123}') \end{array} \right]$$

$$\text{num2} = V_{dc} \times \left[\begin{array}{l} (S_{y2}' + S_{y1}') \times (S_{b2}' + S_{b1}' + S_{123}') \\ - (S_{b2}' + S_{b1}') \times (S_{y2}' + S_{y1}' + S_{123}') \end{array} \right]$$

$$\text{num3} = V_{dc} \times \left[\begin{array}{l} (S_{r2}' + S_{y2}') \times (S_{b2}' + S_{b1}' + S_{123}') \\ - (S_{b2}' + S_{y2}') \times (S_{r2}' + S_{r1}' + S_{123}') \end{array} \right]$$

Using the expression (1)-(7), the analytical waveform of pole voltages, phase voltages and common mode voltage can be obtained.

III. CONTROL SCHEME

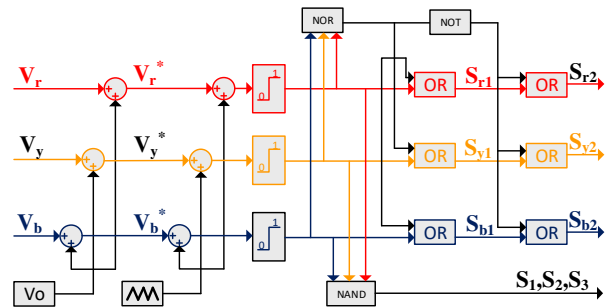


Fig.4 Proposed PWM modulator.

Table.1 Switching Sequence

S_{r1}	S_{r2}	S_{y1}	S_{y2}	S_{b1}	S_{b2}	S_1	S_2	S_3	V_{cm}
1	0	0	1	0	1	1	1	1	$V_{dc}/3$
1	0	1	0	0	1	1	1	1	$2/3 * V_{dc}$
1	0	0	1	1	0	1	1	1	$2/3 * V_{dc}$
0	1	0	1	1	0	1	1	1	$V_{dc}/3$
0	1	1	0	1	0	1	1	1	$2/3 * V_{dc}$
0	1	1	0	0	1	1	1	1	$V_{dc}/3$
1	1	1	1	1	1	0	0	0	$V_{dc}/3$

The implementation of the proposed MDPWM is discussed. The overall block diagram for the proposed PWM is shown in Fig.4. where V_r , V_y , and V_b are the original sinusoidal reference signals, V_0 is the zero-sequence signal, V_0 is calculated via the magnitude test as follows

$$V_0 = \left[\text{sign}(V_{\min}) \right] \left(\frac{V_{dc}}{2} \right) - V_{\min}$$

where V_{\min} is the original sinusoidal reference (V_r , V_y , or V_b) with the minimum magnitude.

After the injection of V_0 , the resultant modulation signals (V_r^* , V_y^* and V_b^*) are then compared with a triangular carrier wave to generate the logic signals.

From the intermediate pulses, the final pulses ' S_{wr1} ', ' S_{wy1} ' and ' S_{wb1} ' are obtained by using OR logic gate as shown in Fig.4. The pulses ' S_{wr2} ', ' S_{wy2} ' and ' S_{wb2} ' are obtained from the pulses ' S_{wr1} ', ' S_{wy1} ' and ' S_{wb1} ' using OR logic and NOT logic gates as shown in Fig.5. In order to generate PWM with one zero vector (S_1, S_2, S_3), simple logic operations where S_r , S_y and S_b are applied NAND logic to generate the desired gating signals. The switching sequence obtained using above control scheme is shown in Table.1

II. SIMULATION RESULT

In order to verify the operation of three-phase two-level inverter which generates two levels in the pole voltage and reduced levels in common mode voltage by incorporating the device junction capacitance (DJC), a simulation is done using MATLAB software. The parameters used for the simulation are $V_{dc}=400$ V and $R_{load}=100$ ohm. To analyze the performance improvement of three-phase inverter a comparative analysis of conventional inverter, H7 inverter and proposed inverter is shown in Fig 4.

The subplots (a)-(c) of Fig.5(i), Fig.5(ii) and Fig.5(iii) shows the waveforms of the pole voltages ' v_{ro} ', ' v_{yo} ' and ' v_{bo} ' for the conventional two-level inverter, H7 two-level inverter and the proposed two-level inverter (considering DJC). The subplots (d)-(f) of Fig.5(i) and Fig.5(ii) shows the waveform of the phase voltages ' v_{rn} ', ' v_{yn} ' and ' v_{bn} '. The maximum value of the output voltage in all the switching combinations is 400V. The subplot (g) of Fig.5(i), Fig.5(ii) and Fig.5(iii) shows the waveform of the common mode voltage ' v_{cm} '. And subplot (h) shows the zoomed version of common mode voltage. The magnitude of ' v_{cm} ' in a conventional two-level inverter is 0 to V_{dc} , in H7 two-level inverter magnitude of ' v_{cm} ' is $V_{dc}/3$ to $2V_{dc}/3$ whereas in proposed the two-level H9 inverter (considering DJC) magnitude of ' v_{cm} ' is $V_{dc}/3$ to $2V_{dc}/3$, but in this method change in common mode voltage with respect to time is less as compared with H7 two level inverter. It is verified the simulation that an additional level is absent in proposed model. The subplot (i) shows the current waveform of two-level inverter and subplots (j) shows the common mode current i_{cmc} of the three different topologies as discussed.

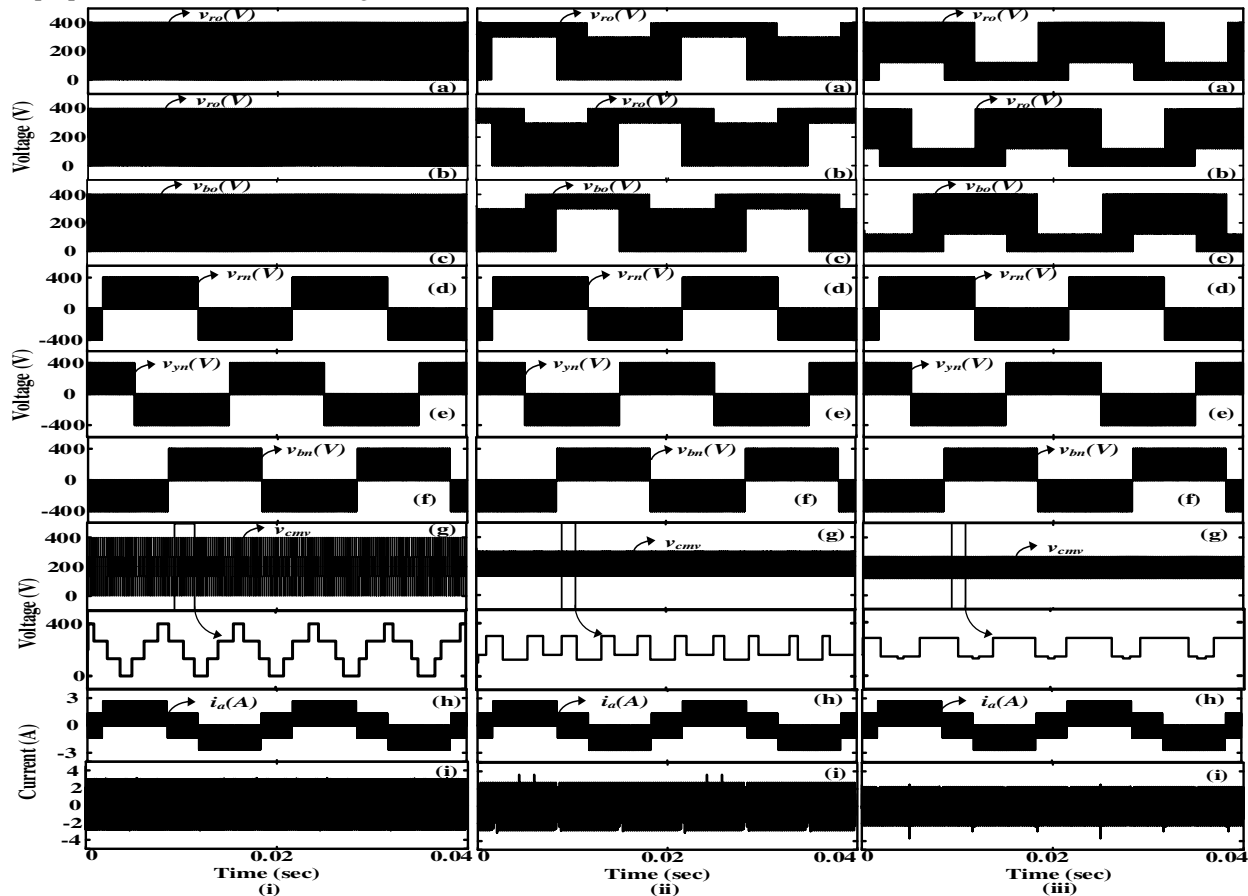


Fig.5 Simulation waveforms of the (i) conventional inverter (ii) two-level inverter H-7, and (iii) proposed two-level inverter H9. (a)-(c) pole voltages ' v_{ro} ', ' v_{yo} ' and ' v_{bo} ', (d)-(f) phase voltages ' v_{rn} ', ' v_{yn} ' and ' v_{bn} ', (g) common mode voltage (h) zoomed version of common mode voltage, (i) current waveform and (j) common mode current i_{cmc}

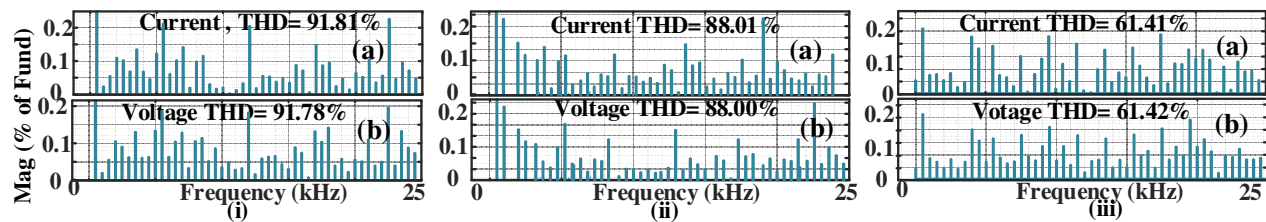


Fig.6 FFT spectrum of the (i) conventional inverter (ii) H7 inverter, and (iii) proposed two-level inverter, (a) phase voltage (b) output current

Fig.6 (a) shows the waveforms of the FFT spectrum in the phase voltage of the (i) conventional inverter (ii) two-level inverter H-7, and (iii) proposed two-level inverter. The THD of the phase voltage of a conventional two-level inverter is around 91.81% whereas for the H7 two-level inverter, the THD is around 88.01% and for the proposed two-level inverter THD is 61.41%. Fig.6 (b) shows the waveforms of the FFT spectrum of the current of (i) conventional inverter (ii) two-level inverter H-7, and (iii) proposed two-level inverter. The THD of the phase voltage of a conventional two-level inverter is around 91.78% whereas for the H7 two-level inverter, the THD is around 88.00% and for the proposed two-level inverter THD is 61.42%.

Conclusion

In conclusion, our research presents a pioneering solution to common mode voltage and current issues in multi-level inverters, offering a promising avenue for advancing power electronics systems' efficiency and reliability. As the demand for high-performance power conversion systems continues to rise, innovative solutions like ours hold the potential to drive substantial progress in energy efficiency and sustainability.

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